

**A Novel, Cost-Effective, High Performance Interface  
System for Distributed Generation**

**Prepared for: Future Energy Challenge**

**Prepared by : University of Minnesota**

**Advisor: Prof. Ned Mohan**

*Ned Mohan*

---

**June 2001**

## **ABSTRACT**

This report presents the design of a 10kW fuel cell interface system to convert the low voltage DC of the fuel cell to a 60Hz AC. The report describes the circuit topology in detail and presents design equations to determine the components of the system. The closed loop control of the system is also discussed and simulation results are presented to verify their behavior. The complete interconnected 10kVA system is also simulated, with different types of loads, to demonstrate the operation of the system.

## Table of Contents

Abstract		i
Table of Contents		ii
List of Figures		iii
Chapter 1	Introduction	i
Chapter 2	Basic Topology	4
Chapter 3	PWM Inverter Design	8
Chapter 4	Novel DC-DC Converter	14
Chapter 5	Closed Loop Control of the DC-DC Converter	23
Chapter 6	Interconnected System	28
Chapter 7	Hardware Prototype	31
Chapter 8	Conclusions	35
References		36

## List of Figures

Fig 2.1. Proposed Topology for the Inverter System	4
Fig. 2.2. Schematic of the proposed DC-DC converter configuration	5
Fig 2.3. Idealized Waveforms for the DC-DC converter	6
Fig. 2.4. Inverter configuration used to achieve 120V/240V AC	7
Fig. 3.1. Circuit Topology of the PWM inverter	8
Fig. 3.2. Block Diagram for the Closed Loop Control of the Half-Bridge PWM Inverter	11
Fig. 3.3: Waveforms for the PWM inverter	13
Fig. 4.1. Schematic of the proposed DC-DC converter configuration	14
Fig. 4.2. Input Current Ripple Waveform at full load	19
Fig. 4.3. Output Waveforms	20
Fig. 4.4. Input Waveforms	20
Fig. 4.5. Circuit Waveforms	21
Fig. 4.6. Transformer Primary Currents	21
Fig. 4.7. ZVS waveforms for full-load	22
Fig. 4.7. ZVS waveforms for minimum-load	22
Fig. 5.1 DC link Capacitor	24
Fig. 5.2. Block Diagram of the Controller for the Hybrid Converter	25
Fig. 5.3. DC-DC Converter Response for a step change in load	26
Fig. 5.4. 120Hz ripple component in the voltage and current	27
Fig. 6.1. SABER schematic of the interconnected system	28
Fig. 6.2. Results for a Resistive load (full load)	29
Fig. 6.3. Results for a Resistive load (10% load)	29
Fig. 6.4. Results for an Inductive load	30
Fig. 6.5. Results for a non-linear load	30

Fig. 7.1. 1.5kW Prototype of the DC DC Converter	31
Fig. 7.2. Transformer Secondary Voltages	32
Fig. 7.3. Input Voltage to the Diode Bridge Rectifier	32
Fig. 7.4. Rectified Output Voltage	33
Fig. 7.5. ZVS characteristics at no load	33

### INTRODUCTION

Utility deregulation has increased the possibilities for distributed energy generation. The market for distributed generation is growing and is expected to reach between 25 and 50GW by 2010 [1]. Advances in technology have lowered the size threshold for economically viable equipment, especially in the case of micro-turbines and fuel cells. Current trends in the United States favor distributed generation due to its increased efficiency and reduced emissions. The increasing sensitivity of electrical equipment and growing concerns over power quality have also prompted many industrial consumers to install medium-sized onsite generation capability.

#### Survey of Existing Interface Topologies

Existing and suggested interface topologies for the intended application can be categorized as follows:

1. Topologies with a 60-Hz Transformer. In these topologies, electrical isolation and voltage matching is provided by means of a 60-Hz transformer at the ac output of the inverter [2]. These have the obvious drawback of cost, size and weight, and losses associated with the 60-Hz transformer.
2. Non-isolated Topologies. In such topologies, the dc source voltage is boosted to a large value, without an isolation transformer and then inverted to interconnect to the utility grid [3]. This topology may not be feasible in many applications where the dc source needs to

grounded at its terminal. Other major drawbacks of these topologies are a large voltage conversion ratio leading to excessive switch ratings and large switch losses.

3. **High-Frequency Isolated Topologies**. There are many variations to these topologies. The common elements to all the topologies are that the dc source voltage is boosted to a higher dc voltage using a high-frequency transformer which provides isolation as well as a voltage step-up. The high-voltage dc is then inverted into the line-frequency ac for utility interconnection by means of a pulse-width-modulated (PWM) inverter. In all cases, the PWM inverter is not soft-switched, thus resulting in switching losses [4]. The dc-dc converter with the high-frequency isolation is usually phase-shift modulated to achieve soft-switch at full load. However, it is not possible to achieve soft-switching below a certain power level (for example, 50% of full-load) without paying an unacceptable penalty in terms of increased conduction losses [5].

### **Proposed Interface System with Extremely Low Switching Losses**

The novel topology interface proposed for this research reduces the switching losses in the DC-DC converter to essentially zero from no-load to full-load, allowing the possibility to achieve very high efficiencies over a full power range and also a very high power density.

### **Scope of the Report**

The proposed topology to convert the low voltage DC to 10V/240V, 60Hz AC is described in Chapter 2. Chapter 3 discusses the operation and design of the PWM inverter, which forms the first stage of the DC-AC inverter system. Simulation results are presented to show the

performance of the system under various load conditions. Chapter 4 describes the novel DC-DC converter configuration, its operation and design. Chapter 5 describes the modifications required in the circuit to reduce the 120Hz ripple current seen by the fuel cell. It also describes the control loop design for the DC-DC converter. Chapter 6 describes the interconnection of the two stages. Simulation results are presented to show the operation of the entire system for various loads. Chapter 7 describes the status of the 1.5kW hardware prototype being built to demonstrate the feasibility of the proposed topology. Finally, the report is concluded in chapter 8, which summarizes the features of the proposed system.

## BASIC TOPOLOGY

This chapter presents the basic topology used to convert the low voltage DC output of the fuel cell to the required 120V/240V, 60Hz split single phase AC. The operation of the circuit under steady state conditions is explained, along with the various features of the proposed system. The advantages of the proposed topology are also discussed.

## Circuit Topology

The block diagram of the proposed DC-AC inverter system is shown in Fig. 2.1.

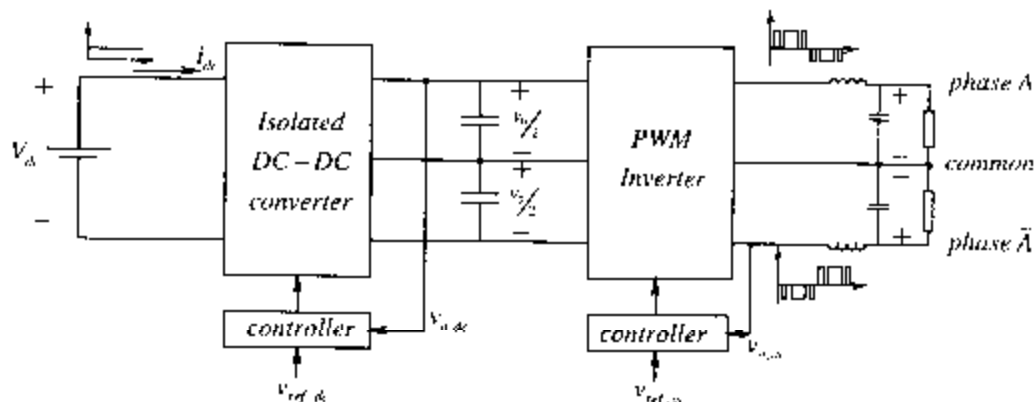


Fig 2.1. Proposed Topology for the Inverter System

The system consists of a DC-DC converter stage with high frequency isolation, a split-capacitor dc link followed by a sinusoidally pulse-width-modulated (PWM) inverter. The inverter utilizes the split dc bus to generate a 120/240V AC output voltage.

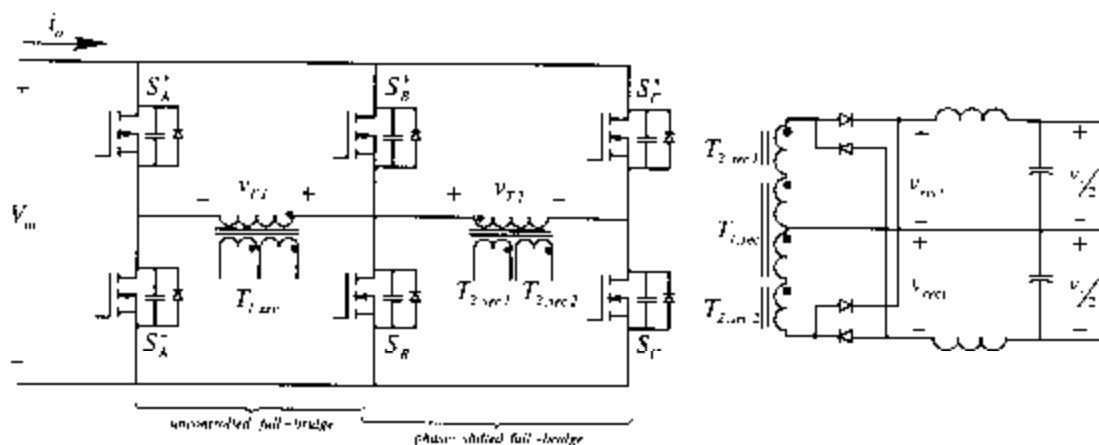
A novel hybrid configuration is proposed for the dc-dc converter, which enables Zero-Voltage Switching (ZVS) for all switches under all operating conditions, enabling efficient operation even at very high switching frequencies [6]. It also results in improved filter waveforms

resulting in significantly reduced filter requirements, enabling a very high power density. Moreover, the topology maintains an equal distribution of the output voltage across the split dc link irrespective of the values of the output capacitors and the loading conditions between the two halves. The proposed dc-dc converter reduces the filter requirement by a factor of *five* (for the input voltage variation specified in the energy challenge) as compared to conventional phase-modulated dc-dc converters used for achieving soft switching.

The inverter configuration utilizes four switches to obtain a 120V/240V system at the output and ensures equal loading for both halves of the DC link under all loading conditions. The control of the DC-DC converter and the PWM inverter are totally de-coupled, enabling the use of simple analog control circuitry, which would reduce the cost of the entire system.

### DC-DC Converter Topology

Fig. 2.2 shows the proposed hybrid configuration for the DC-DC converter stage of the inverter system [7]. It is a combination of an uncontrolled full-bridge and a phase-shift-controlled full-bridge. The uncontrolled sections consist of the switches  $S_A^+$ ,  $S_A^-$ ,  $S_B^+$  and  $S_B^-$  and the transformer  $T_1$ , which always operates with full pulse width. The controlled section consists of switches  $S_C^+$



**Fig. 2.2. Schematic of the proposed DC-DC converter configuration**

$S_u$ ,  $S_c^+$  and  $S_c^-$  and the transformer  $T_2$ . The six switches have a combined rating equal to the combined ratings of the four switches in a conventional full-bridge converter. All switches are operated at constant switching frequency and a fixed 50% duty ratio.

The phase difference between the legs B and C is controlled to achieve output voltage control. The outputs of the two sections are added at the secondary, rectified and filtered. The secondary-side configuration combining a full-bridge rectifier with a center-tapped transformer results in equal voltage sharing between the two halves of the output capacitor under all loading conditions. The idealized waveforms for the proposed DC-DC converter topology are shown in Fig. 2.3. As it can be seen, the output voltage and input current waveforms are much closer instantaneously to their average values, reducing filter requirements. For a 1:2 input voltage requirement, the requirements on the output inductor rating and the input capacitor ripple current rating are reduced by a factor of approximately three.

Another advantage of the proposed DC-DC converter configuration is that it can achieve a ZVS under light load conditions also, without serious conduction loss penalty as in conventional phase modulated converters. Since the system needs to operate at varying output power conditions,

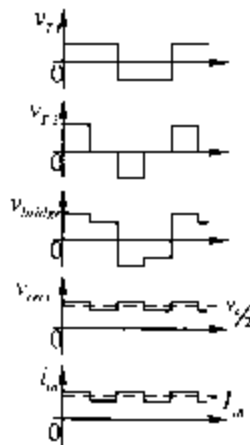


Fig 2.3. Idealized Waveforms for the DC-DC converter

soft switching under all operating conditions is an important requirement, if the converter is to operate efficiently.

### Inverter Configuration

Fig. 2.4 shows the inverter configuration used to achieve a 120V/240V output voltage. The control strategy is similar to a standard PWM inverter with the gate signals for the inverter being generated by the comparison of a sine wave with a ramp. The configuration maintains equal loading on the 2 capacitors of the DC link even if one of the phases is not loaded and thus simplifies the choice of the capacitor current ratings. Thus, this topology can be used under all loading conditions, as is the case for any inverter system supplying a house or building.

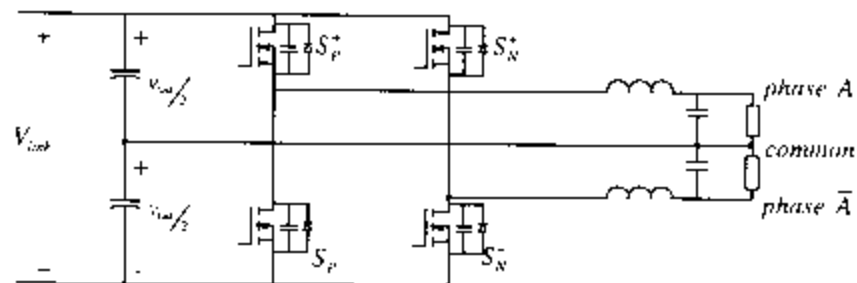


Fig. 2.4. Inverter configuration used to achieve 120V/240V AC

## PWM INVERTER DESIGN

This chapter presents the analytical design of the power stage of the PWM inverter used to obtain the required 120V/240V, 60Hz AC output from the split DC link. The design of the closed loop controller required to maintain the output voltage under all load conditions is also presented. Simulation results showing the performance of the PWM inverter in both open loop and closed loop modes of operation are presented.

## Design of the Power Stage

The circuit diagram of the PWM inverter is shown in Fig. 3.1.

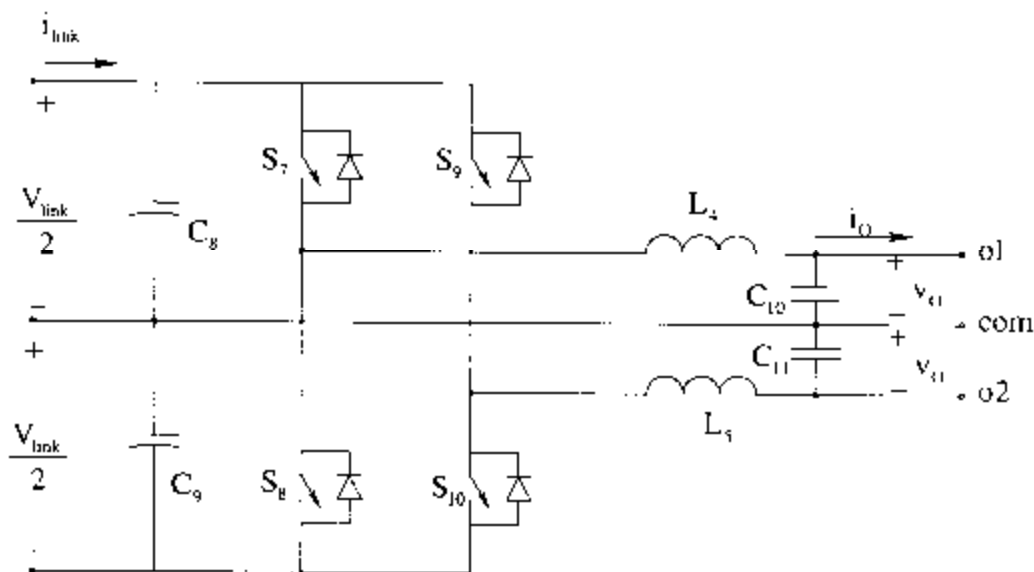


Fig. 3.1. Circuit Topology of the PWM inverter

The nominal output current  $I_o$  is

$$I_o (rms) = \frac{S_{output}}{V_{o,max}} = 41.67 A . \quad (3.1)$$

$$\hat{I}_o (peak) = \sqrt{2} I_{rms} = 59 A .$$

For the purpose of choosing the semiconductor devices, the peak output current is limited to 60A.

### Output Filter Design

Assuming a constant output voltage during a switching cycle (switching frequency  $f_s = 20kHz$ ), the worst-case peak-to-peak ripple current in the inductor can be expressed as,

$$\Delta i_{p-p, worst\ case} = \frac{1}{2} \left( \frac{V_{link}}{2 L f_s} \right) . \quad (3.2)$$

Assuming a peak current ripple equal to 10% of the maximum nominal output current,

$$\Delta i_{p-p, worst\ case} = \frac{1}{2} \left( \frac{450}{2 \times L \times 20,000} \right) = 6 A \quad (3.3)$$

$$\Rightarrow L = 937.5 \mu H .$$

The voltage ripple across the output capacitor, caused by the inductor ripple current can be expressed as,

$$\Delta v_{p-p} = \frac{1}{C} \int_{\frac{T}{2}}^{\frac{3T}{2}} i_{L,ripple} dt . \quad (3.4)$$

Choosing an output voltage ripple equal to 1% of the maximum output voltage,

$$\Delta v_{p-p} = \frac{1}{2C} \left( \frac{\Delta i_L}{2 f_s} \right) = 3.4 V \quad \Rightarrow C = 22 \mu F . \quad (3.5)$$

Splitting the output filter between the two phases,

$$L_s = L_r = 937.5 \mu H, 42 A @ 60 Hz$$

$$C_s = C_r = 44 \mu F, 150 VAC . \quad (3.6)$$

### Switch Ratings

The maximum voltage across any switch of the PWM inverter is 450V and the rms current through it is approximately 32A. A 600V, 96A switch is chosen so that

- It can withstand voltage spikes due to stray inductances.
- It can carry the peak output current after being derated for the increased temperature of operation.

MOSFETs are found to be better than IGBTs for the present application, since the large turn-off times of the IGBTs would increase the switching losses at the chosen frequency of operation.

Each switch of the inverter is chosen to be made up of two IXFN44N60 MOSFETs in parallel, giving a total current rating of 88A. Each MOSFET has the following parameters:

$$t_{on} = 50ns$$

$$t_{off} = 50ns$$

$$r_{on} = 0.13\Omega$$

$$\text{voltage drop in body diode} = 1.3V$$

The total conduction and switching power loss in the switches, using the parameters of the chosen MOSFET is

$$P_{loss, switches} = \underbrace{266W}_{\text{conduction loss}} + \underbrace{58W}_{\text{switching loss}} = 324W \quad (3.7)$$

The efficiency of the PWM inverter stage is

$$\eta_{inv} = \frac{10000}{10324} \times 100 = 96.8\% \quad (3.8)$$

### **Feedback Controller Design**

Since the system is being designed for a 50% unbalance in the load (one phase is at full load and the other phase is at minimum load), it is necessary to control each half bridge inverter

individually. This section discusses the control loop design for one half-bridge inverter. The complete PWM inverter will consist of two such half bridges, connected appropriately.

The controller for the PWM inverter has to ensure that the output voltage is sinusoidal voltage of fixed amplitude and frequency, irrespective of the load. Given the vast variation that is possible in the load as well as in the type of load (resistive, reactive and nonlinear), it is difficult to design a controller based on the bode plots of the system. The use of a feedforward controller to eliminate the effect of the load current on the output voltage would simplify the control loop design of the PWM inverter greatly. Fig. 3.2 shows the block diagram of the control structure used to regulate the output voltage.

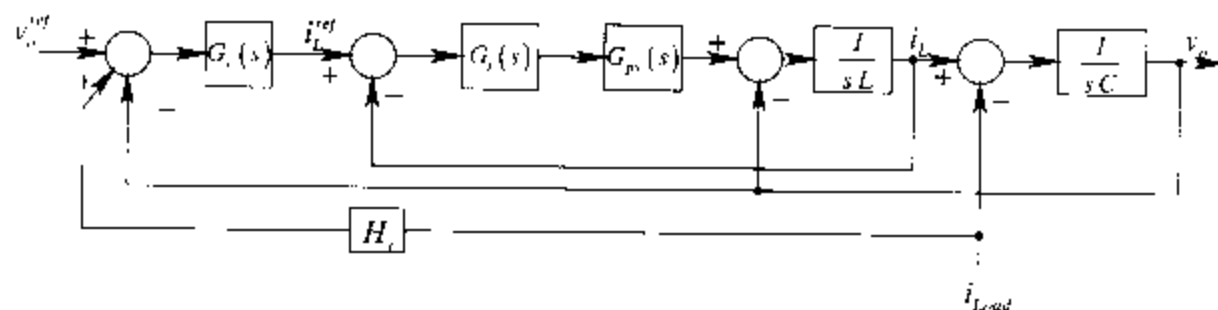


Fig. 3.2. Block Diagram for the Closed Loop Control of the Half-Bridge PWM Inverter

The transfer function of the system shown above is

$$v_o \left( 1 + \frac{G_f G_{pr}}{sL} + \frac{1}{s^2 LC} \right) = (v_o^{ref} - v_o) \frac{G_c G_f G_{ps}}{s^2 LC} + i_{Load} \left( \frac{H_f G_c G_f G_{pr}}{s^2 LC} - \frac{G_f G_{ps}}{s^2 LC} - \frac{1}{sC} \right). \quad (3.9)$$

From (3), it can be seen that by properly choosing the feedforward transfer function  $H_f$ , it is possible to eliminate the effect of the load current on the output voltage. Thus, choosing

$$H_f(s) = \frac{1}{G_c} + \frac{sL}{G_c G_f G_{ps}}, \quad (3.10)$$

the output voltage transfer function reduces to

$$v_o = (v_a^{ref} - v_o) \frac{G_v G_i G_{pr}}{s^2 LC + sC G_i G_{pr} + 1} \quad (3.11)$$

The power stage transfer function  $G_{pr}$  can be considered to be a pure gain, since the response time of the power electronic circuitry is much smaller than the response time of the output LC filter. Eqn. 3.11 indicates that choosing simple gains for the voltage and the current controllers would be sufficient to achieve the required performance. Choosing a crossover frequency of 2.5kHz and a phase margin of  $60^\circ$ , the parameters of the feedback controller are

$$\begin{aligned} G_v &= 0.48 \\ G_i &= 0.1863 \\ H_f &= 2.08 + \frac{s}{(2\pi) \times 1670} \end{aligned} \quad (3.12)$$

The feedforward controller turns out to be a differentiator, which would amplify high frequency noise. Since the load current would be in the low frequency region (60Hz and its odd multiples), adding a high frequency pole to the system would not affect the system response to the load current. The pole would damp out the effects of the zero at high frequencies. Thus, a practical feedforward controller would be

$$H_f = \frac{2.08 + \frac{s}{(2\pi) \times 1670}}{1 + \frac{s}{(2\pi) \times 10,000}} \quad (3.13)$$

### Simulation Results

Fig. 3.3 shows the simulation results for the 10kVA PWM inverter, under feedback control. The load initially is a resistive 10kW load, which is changed to an inductive load of 10kVA at 0.6pf

at 50ms. As it can be seen from the waveforms, the closed loop controller is able to maintain the voltage across the load at all times.

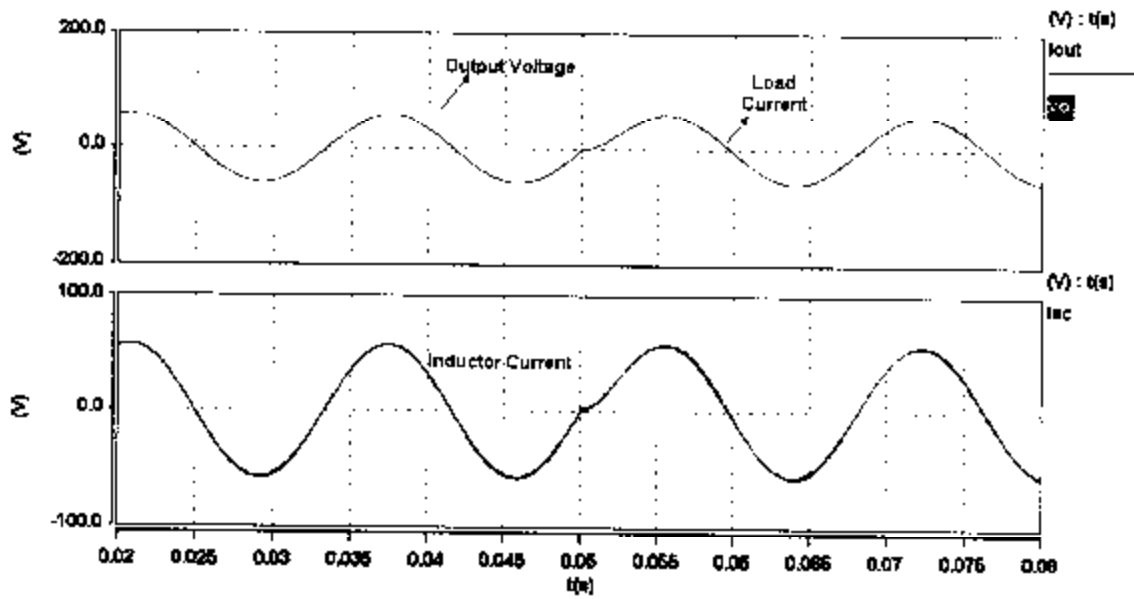


Fig. 3.3: Waveforms for the PWM inverter

NOVEL DC-DC CONVERTER

This chapter presents the analytical design of the power stage of the DC-DC converter used to step up the low voltage DC to high voltage DC and provide a split DC link. The design of the resonant circuit components required to achieve ZVS from full load to minimum load is also presented. Simulation results showing the performance of the converter in open loop are presented.

Design of the DC-DC Converter

The circuit diagram of the novel DC-DC converter is shown in Fig. 4.1.

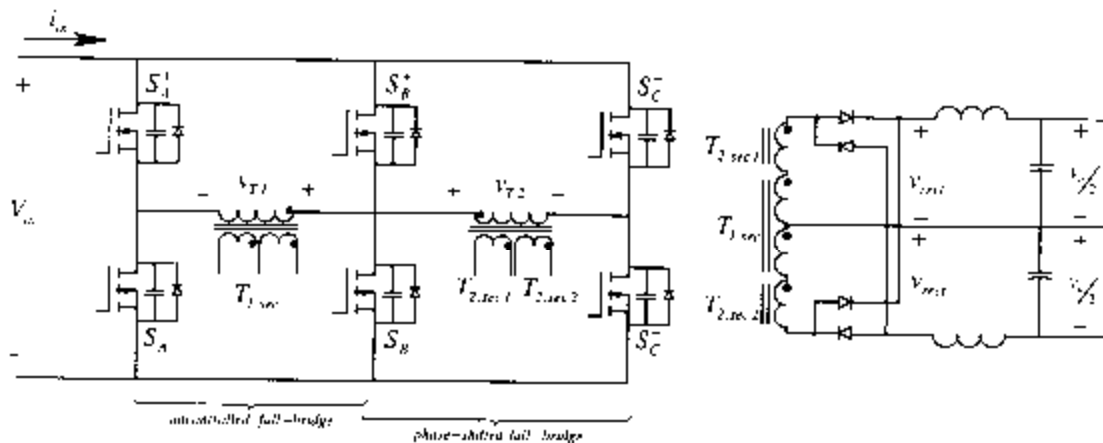


Fig. 4.1. Schematic of the proposed DC-DC converter configuration

The nominal output current  $I_o$  is

$$I_o = \frac{S_{output}}{\eta_{inv} V_o} \approx 24 A, \quad (4.1)$$

assuming that the total output voltage is 450V and using a 96% efficiency for the inverter (as computed in chapter 3).

Thus, each diode on the secondary side will have an average current rating of 12A. Choose DSEI19-06AS for the four secondary diodes (600V, 20A diodes). Using the parameters of these diodes, the total loss computed at a switching frequency of 50kHz is

$$P_{\text{loss, diodes}} = \underbrace{72W}_{\text{conduction losses}} + \underbrace{20W}_{\text{switching losses}} = 92W, \quad (4.2)$$

### Transformer Turns Ratio Selection

The turns ratios of the two transformers are chosen based on the input voltage variation and the required output voltage. Since the voltage across transformer T1 is uncontrolled and the voltage across transformer T2 is controlled, the requirements are

- At the minimum input voltage, the sum of the two transformer voltages is equal to the output voltage  $\rightarrow V_{i,\text{min}} n_1 + V_{i,\text{min}} n_2 = V_o$
- At the maximum input voltage, all the output voltage is due to transformer T1 alone.  $\Rightarrow V_{i,\text{max}} n_1 = V_o$

For the given parameters (input voltage variation is from 42V to 72V and output voltage is 450V),

$$\begin{aligned} n_1 &= 6.25 \\ n_2 &= 4.5. \end{aligned} \quad (4.3)$$

The input voltage to output voltage relationship in steady state is

$$V_o = V_{i1} n_1 + d(V_{i2} n_2) \quad (4.4)$$

The transformers T1 and T2 have 2 secondaries each, with turns ratios of  $\frac{n_1}{2}$  and  $\frac{n_2}{2}$  respectively.

### Main Switch Ratings

The switches in the three legs of the primary carry the following currents:

$$\begin{aligned} \text{Leg A : } n_1 I_o &= 106 \text{ A rms.} \\ \text{Leg B : } (n_1 + n_2) I_o &= 182 \text{ A rms.} \\ \text{Leg C : } n_2 I_o &= 76 \text{ A rms.} \end{aligned} \quad (4.5)$$

Thus, the following combination of MOSFETs is chosen to achieve the above current ratings.

Leg A: *Three* IXFH75N10 in parallel

Leg B: *Five* IXFH75N10 in parallel

Leg C: *Two* IXFH75N10 in parallel

The IXYS MOSFET IXFH75N10 has the following parameters:

$$\begin{aligned} t_{on}, t_{off} &= 50 \text{ ns} \\ r_{ds,on} &= 0.02 \Omega \\ V_{ds,cr} &= 1.75 \text{ V} \end{aligned} \quad (4.6)$$

### Zero Voltage Switching

The mechanism of zero voltage switching in the proposed hybrid converter is similar to that of the conventional PMC, in that it relies on the transformer primary current to charge/discharge the appropriate switch capacitance just prior to turn-on.

In the new configuration, achieving ZVS for the right leg (leg C) is simple since the load current does not change direction during the transition. The magnetizing current of the transformer T1 is increased in order to enable ZVS for legs A and B. However, since this magnetizing current does not significantly increase the rms currents through the switches, the total conduction losses do not increase as in the case of the conventional PMC.

### Left Leg Transitions

Consider the switches  $T_A^+$  and  $T_B^-$  gated on initially. The left leg transition begins when  $T_A^+$  is turned off. In the new configuration, when both switches are turned off, the sum of the two secondary voltages becomes negative only when the voltage across  $T_A^+$  reaches  $V_{start}$  given by

$$V_{start} = V_{in} \frac{n_1}{2(n_1 + n_2)} \quad (4.7)$$

For the current design,  $V_{start} = 14V$ . The capacitances are chosen such that in the turn off time for the MOSFET, the voltage across the mosfet reaches  $V_{start}$ . Thus, the first design equation is

$$\frac{\{\hat{I}_{max} + (n_1 + n_2)I_o\}}{4C} t_{off} = V_{start} \quad (4.8)$$

where  $\hat{I}_{max}$  is the peak of the magnetizing current. (Note: Eqn. 4.8 is written for the mosfets in leg B).

The second equation is that the voltage across the capacitor reaches zero in one-fourth the resonant interval.

$$48 \leq \left\{ \hat{I}_{max} + (n_1 + n_2)I_o \right\} \sqrt{\frac{L_{eq}}{2C}} + V_{start} \quad (4.9)$$

where  $L_{eq} = \frac{L_{lk,1} n_1^2 + L_{lk,2} n_2^2}{(n_1 + n_2)^2}$ . ( $L_{lk,1}$  and  $L_{lk,2}$  are leakage inductances of the two transformers

referred to their secondaries).

The final equation establishes the blanking time ( $t_b$ ) between the mosfets, under minimum load conditions (10% of full load).

$$\frac{\{\hat{I}_{max} + 0.1(n_1 + n_2)I_o\}}{4C} t_{off} + \frac{\{\hat{I}_{max} + 0.1(n_1 + n_2)I_o\}}{2C} (t_b - t_{off}) = V_{in} \quad (4.10)$$

Using the above three equations, with a blanking time of 500ns, the following parameters are obtained.

$$\text{Leg A : } C = 163 \text{ nF}$$

$$\text{Leg B : } C = 260 \text{ nF}$$

$$\text{Magnetizing current peak : } \hat{I}_{max} = 32.25 \text{ A.}$$

The capacitance of Leg C is based on achieving ZVS under minimum-load conditions. Thus

$$\text{Leg C : } C = 50 \text{ nF.}$$

### Output Filter Design

Assuming a constant output voltage during a switching cycle (switching frequency  $f_s = 50\text{kHz}$ ).

the worst-case peak-to-peak ripple current in the inductor can be expressed as,

$$\Delta i_{p-p, \text{worst case}} = \frac{\left( V_o - n_f \frac{V_{in}}{2} \right) (I - D) \frac{I_f}{2}}{L_r} \quad (4.11)$$

For the given input voltage variation, the worst case current ripple occurs at  $V_{in} = 55\text{V}$ .

Assuming a peak current ripple equal to 10% of the maximum nominal output current,

$$L = 660 \mu\text{H}. \quad (4.12)$$

The voltage ripple across the output capacitor, caused by the inductor ripple current can be expressed as,

$$\Delta v_{p-p} = \frac{I}{C} \int_{\frac{t}{T}}^{\frac{t+T}{T}} i_{L, \text{ripple}} dt. \quad (4.13)$$

Choosing an output voltage ripple equal to 1% of the maximum output voltage,

$$C = 3 \mu\text{F}. \quad (4.14)$$

Splitting the output filter between the parts of the DC link,

$$\begin{aligned} L_d = L_n &= 660\mu H, 24A \\ C_d = C_n &= 3\mu F, 300VDC. \end{aligned} \quad (4.15)$$

### Input Filter

Since the topology doubles the switching frequency component of the input current, the input filter has to be designed for 100kHz. For an input L-C filter, the inductor current to input current transfer function is given by

$$\frac{i_L}{i_m} = \frac{1}{1 + s^2 LC} \quad (4.16)$$

The input current ripple of the converter is shown in Fig. 4.2. The fundamental component of the waveform is 56.65A. To achieve a 10% high frequency current ripple in the input current (20A), choose,

$$\begin{aligned} L &= 136.8nH, 210A \\ C &= 500\mu F, 100VDC. \end{aligned} \quad (4.17)$$

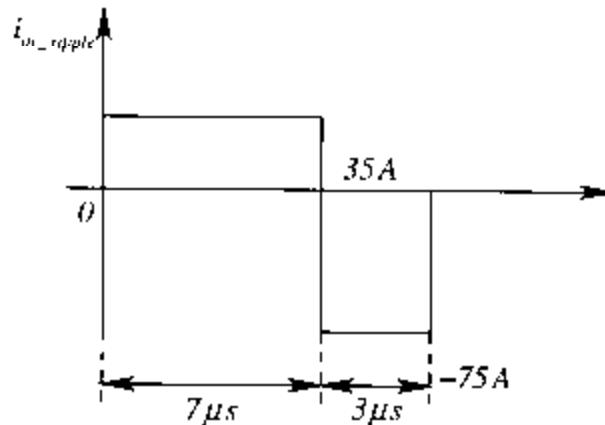


Fig. 4.2. Input Current Ripple Waveform at full load

## Simulation Results

Fig. 4.3 shows the waveforms for the output current and output voltage. The peak-to-peak ripple in the waveforms are far less than the designed values since the design was done for the worst case, and the results being presented are for the nominal input voltage of 48V.

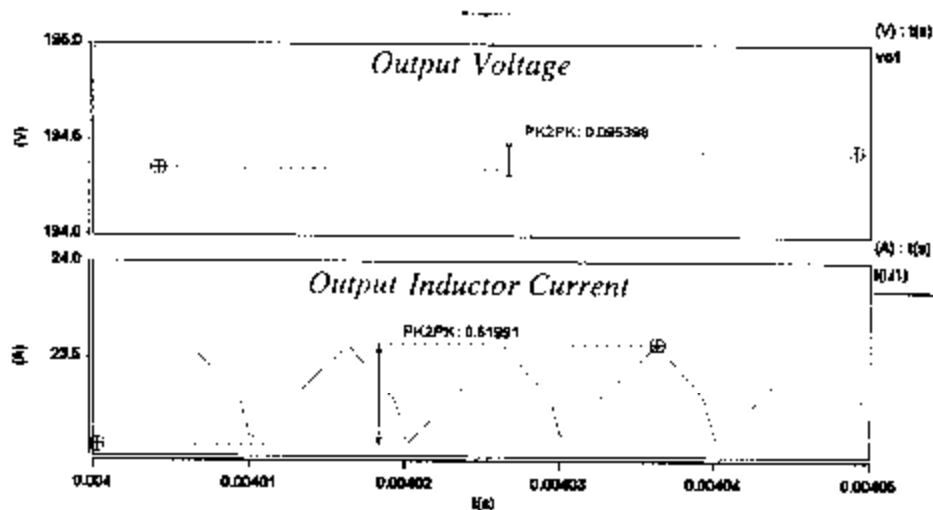


Fig. 4.3. Output Waveforms

Fig. 4.4 shows the input voltage and input current waveforms. The input current ripple is within the specified limits.

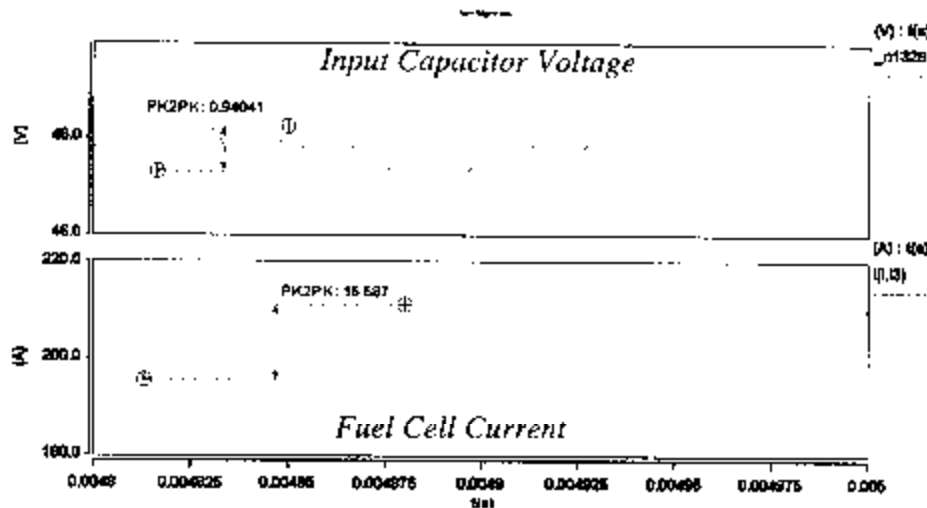


Fig. 4.4. Input Waveforms

Fig. 4.5 shows the actual input current of the DC-DC converter and the output voltage at the end of the diode bridge. As it can be seen, the actual waveforms are close to the DC value since the values do not go to zero for a long period of time.

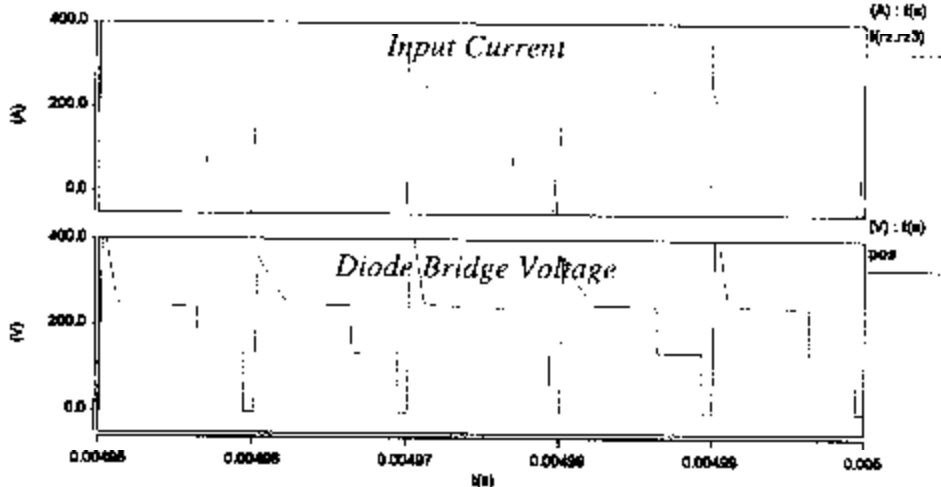


Fig. 4.5. Circuit Waveforms

Fig. 4.6 shows the transformer current waveforms. The primary current of transformer T1 is found to have significant magnetizing current as required, whereas transformer T2 does not. The magnetizing current of the transformer increases the rms value of the primary current by only 1%, thus achieving zero-voltage switching at minimum increase in conduction losses.

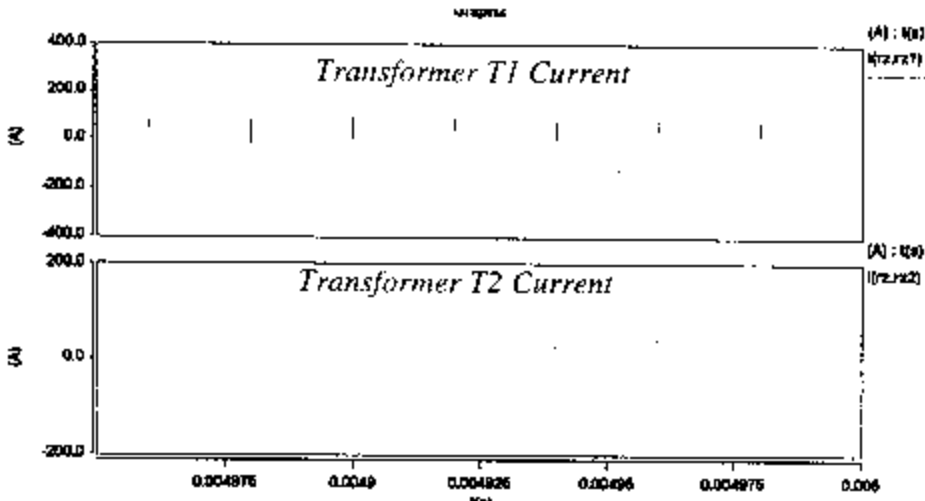


Fig. 4.6. Transformer Primary Currents

Fig. 4.7 shows the ZVS waveforms for full load and Fig. 4.8 shows the same waveforms for minimum load conditions.

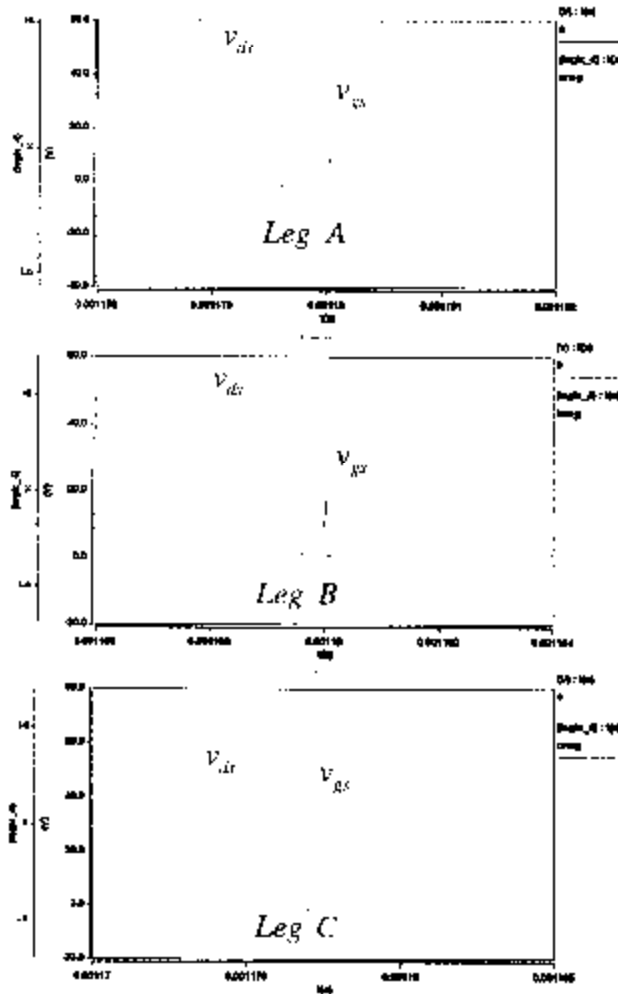


Fig. 4.7. ZVS waveforms for full-load

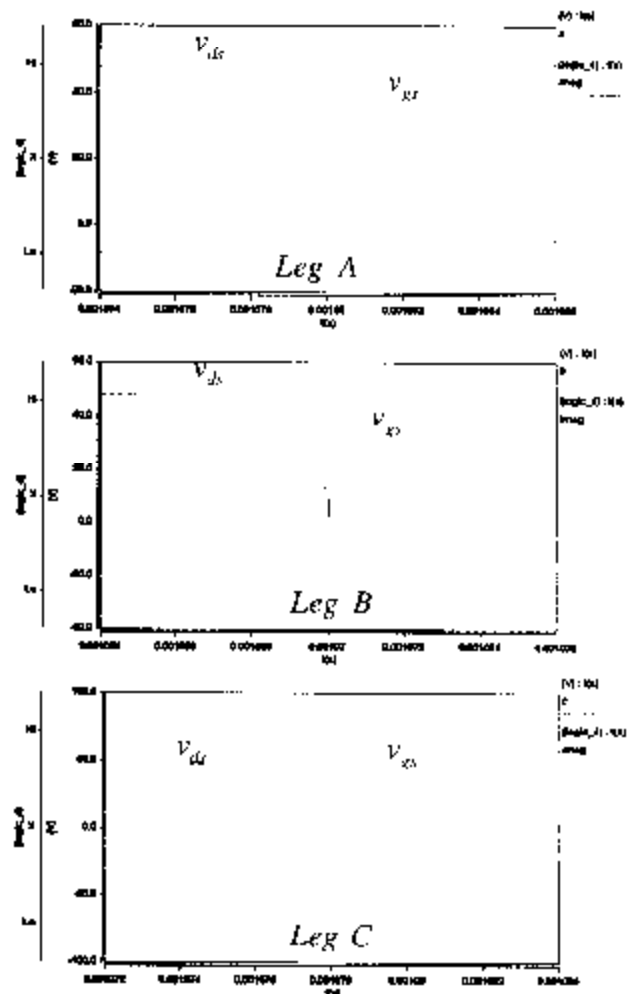


Fig. 4.8. ZVS waveforms for minimum-load

### CLOSED LOOP CONTROL OF THE DC-DC CONVERTER

This chapter presents the modifications in the design required to account for the 120Hz ripple in the output power. The feedback controller design for the DC-DC converter is also discussed and results are presented to show the performance of the controller.

#### Low Frequency Ripple

Since the load is a single phase load, the input power of the PWM inverter will have a 120Hz component. However, since it is preferable to draw a constant power from the fuel cell, energy storage is necessary within the circuit topology to store the difference between the input and output energies.

In this particular topology, the energy storage element is the DC link capacitor. The DC link capacitors are resized such that they store the difference in energies with only a small voltage ripple at its terminals.

In order to maintain a constant input current, the feedback controller of the DC-DC converter is designed to be a cascaded control structure with an inner current loop and an outer voltage loop. The bandwidth of the voltage loop is chosen to be very small so that it attenuates the 120Hz component of the sensed output voltage, providing a near constant current reference to the inner current loop.

## Design of the 120Hz Filter

Fig. 5.1 shows the DC link capacitor and the currents associated with it.

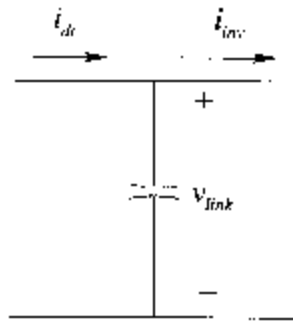


Fig. 5.1. DC link Capacitor

The instantaneous input power to the PWM inverter is

$$p_{in}(t) = v_{link}(t) \times i_{inv}(t) = P - P \cos(2\omega t), \quad (5.1)$$

where  $\omega = 2\pi \times 60$ .

An approximate solution to the capacitor voltage and inverter current waveforms is

$$\begin{aligned} v_{link}(t) &= V_d + \Delta v \cos(2\omega t) \\ i_{inv}(t) &= I_d + \Delta i \cos(2\omega t). \end{aligned} \quad (5.2)$$

Multiplying the instantaneous voltage and current waveforms and equating the result to Eq. 5.1 gives

$$\begin{aligned} V_d I_d &= P \\ \Delta v I_d + \Delta i V_d &= P. \end{aligned} \quad (5.3)$$

Assuming a 10% variation in the DC link voltage, the current ripple at full load is computed to be

$$\Delta i = 20 \text{ A}. \quad (5.4)$$

The capacitor selection is dominated by the ripple current specification rather than the capacitor value. Hence, the capacitance value chosen for this purpose is

$$C = 4950 \mu\text{F}. \quad (5.5)$$

(Note: The capacitor selection is obtained from the ripple current ratings on the Cornell Dubilier website;)

### Control Loop Design

The block diagram of the controller for the DC-DC converter is shown in Fig. 5.2.

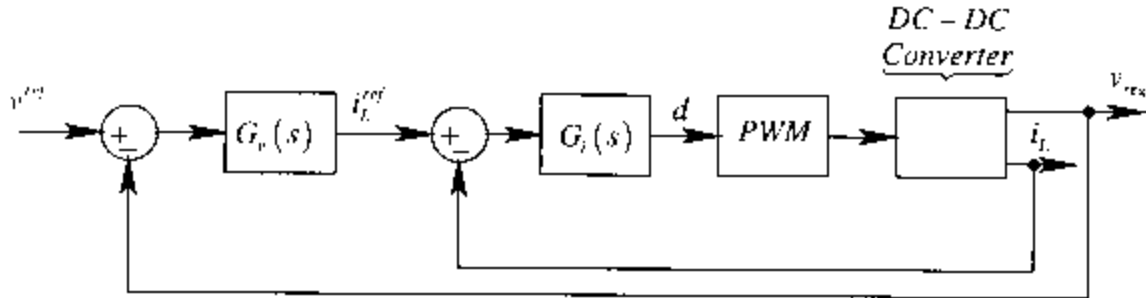


Fig. 5.2. Block Diagram of the Controller for the Hybrid Converter

#### Current Controller

The small signal model of the DC-DC converter is similar to that of a buck converter. The current loop controller is designed with a crossover frequency of 5kHz and a phase margin of  $80^\circ$ . A type 2 [8] controller is designed for the system. The transfer function of the current controller is

$$G_i(s) = \frac{80}{s} \frac{\left( 1 + \frac{s}{(2\pi) \times 133.8} \right)}{\left( 1 + \frac{s}{(2\pi) \times 186529} \right)} \quad (5.6)$$

#### Voltage Controller

The voltage controller has to reject the 120Hz component of the sensed output voltage and so a very low crossover frequency is chosen for the controller. The condition on the controller is

$$|G_c(s)|_{\omega=2\pi 120} = \frac{i_{ref}|_{\omega=2\pi 120}}{V_o|_{\omega=2\pi 120}} \quad (5.7)$$

The 120Hz ripple current component in the current reference is chosen to be 5% of the full load current (1.2A). Choosing a single pole transfer function as the controller, the controller transfer function with the largest possible bandwidth (obtained using iterations) is

$$G_c(s) = \frac{2}{1 + \frac{s}{2\pi(10)}} \quad (5.8)$$

The response of the DC to DC converter to a power load of the form shown in Eq. 5.1 is shown in Fig. 5.3. A step change in the load from 10kW to 1kW is applied at t=1.5s. The controller is able to respond to the change and maintain a near constant DC current.

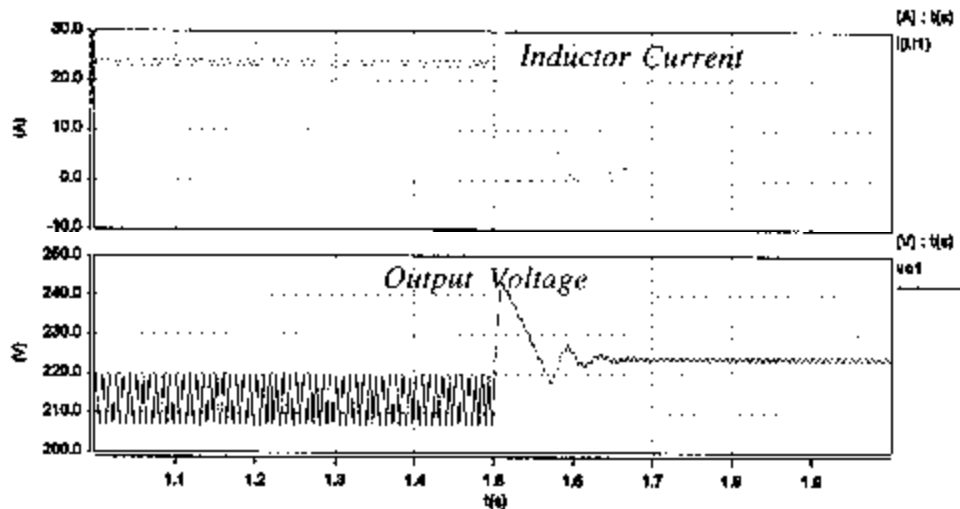


Fig. 5.3. DC-DC Converter Response for a step change in load

Fig. 5.4 shows the DC link voltage ripple and inductor current ripple under full load conditions. The inductor current ripple is found to be 6.5%, close to the 5% desired.

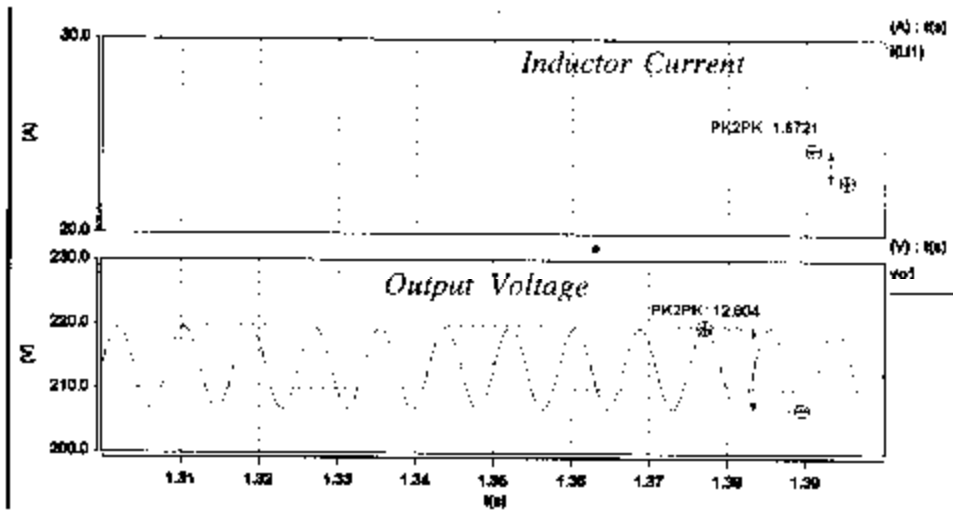


Fig. 5.4. 120Hz ripple component in the voltage and current

## INTERCONNECTED SYSTEM

This chapter presents the results for the interconnected system under all load conditions. Since the points of interest in the interconnected system are the control loop behavior and the low frequency ripple, average models are used to simulate the interconnected system.

## SABER Implementation

The SABER [9] implementation of the entire system is shown in Fig. 6.1. The system consists of an average model for the six switch DC-DC converter and the average models for each half-bridge PWM inverter. The inverter modules also include the feedback loop described in chapter 3. The DC-DC feedback loop is shown in the figure. The two inverters are given sinusoidal references which are out of phase with each other, to generate the split single phase output.

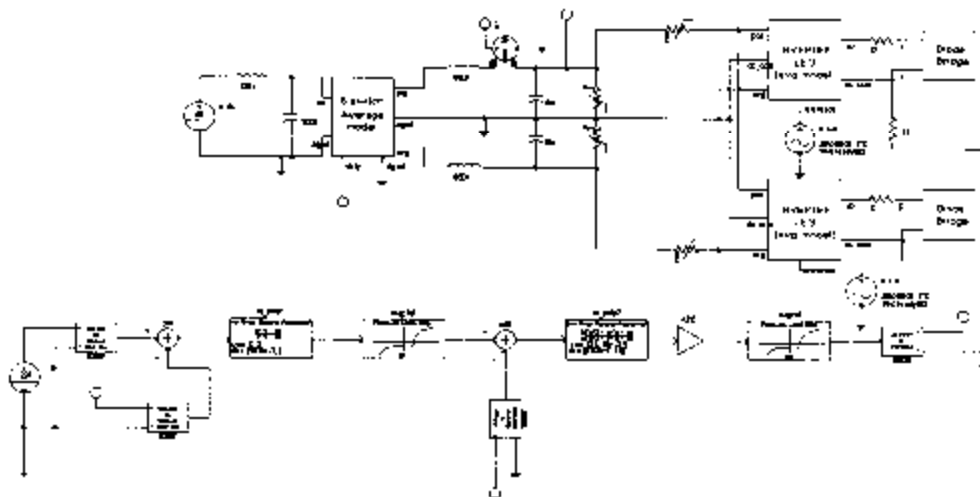


Fig. 6.1. SABER schematic of the interconnected system

### Results for Resistive Loads

Figs. 6.2 and 6.3 show the results obtained for a resistive load at the inverter output, for full load and 10% load respectively.

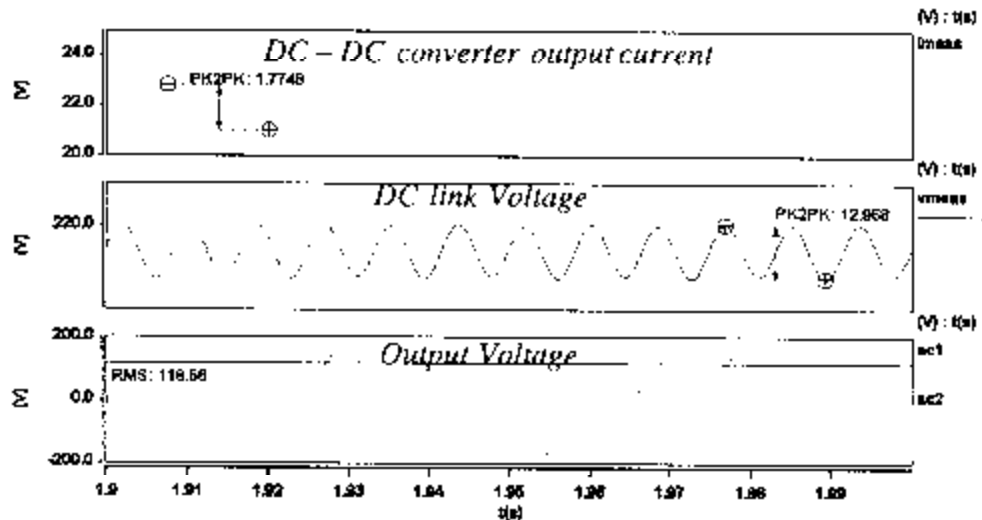


Fig. 6.2. Results for a Resistive load (full load)

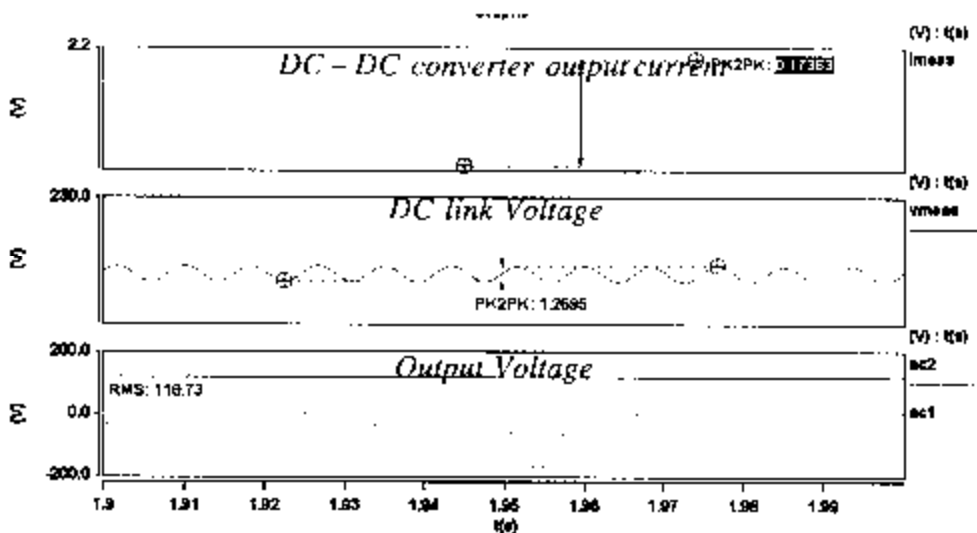


Fig. 6.3. Results for a Resistive load (10% load)

### Results for an Inductive Load

Fig. 6.4 shows the results for an inductive load. The load is a 10kVA load at 0.6pf lagging.

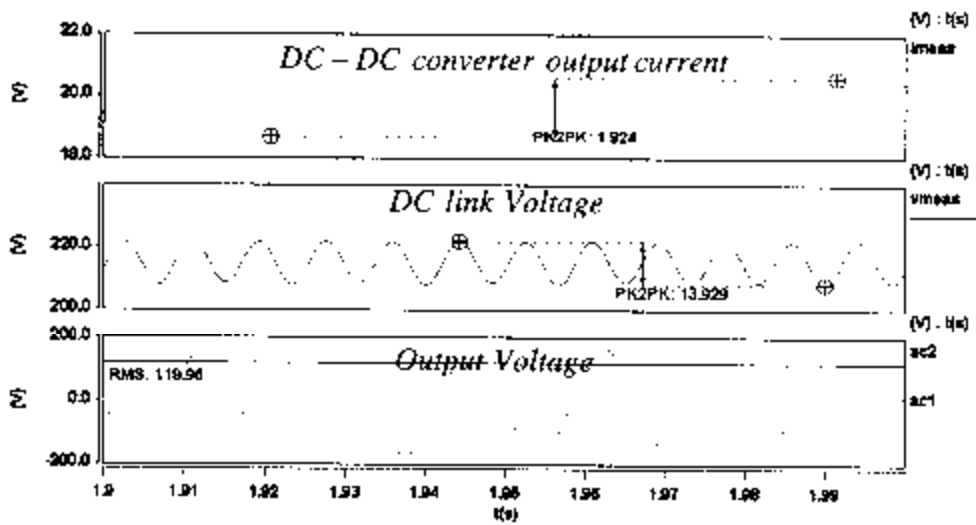


Fig. 6.4. Results for an Inductive load

### Results for a Non-Linear Load

The system was also tested for a single phase diode bridge load. The results are shown in Fig. 6.5.

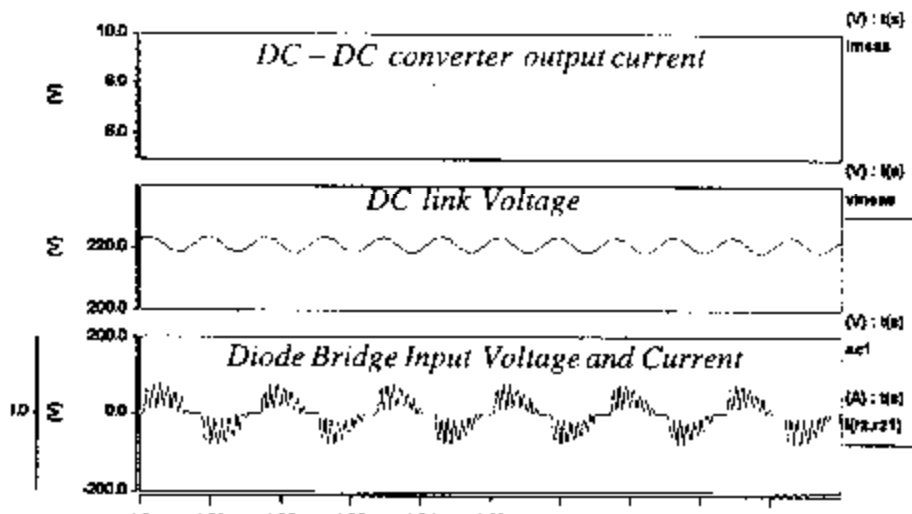


Fig. 6.5. Results for a non-linear load

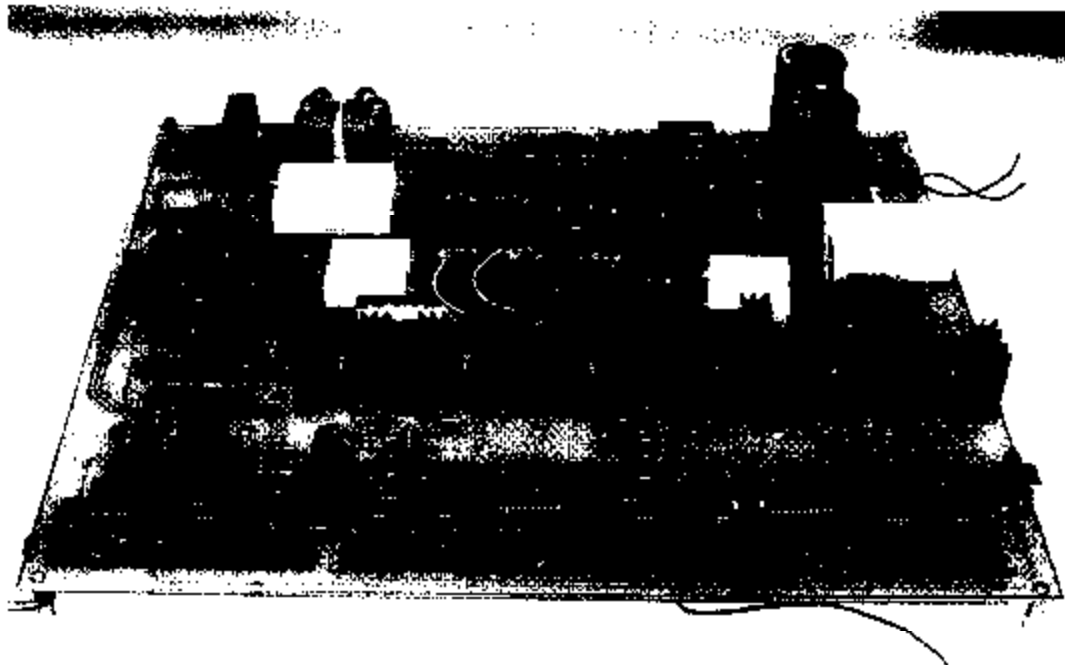
For all the cases, it is found that the system is able to respond to the load changes and is able to adjust depending on the type of the load.

**HARDWARE PROTOTYPE**

A 1.5kW hardware prototype is under construction at the University of Minnesota to demonstrate the feasibility of the proposed approach. The DC-DC converter part of the proposed topology has been built and is in the testing phase. The PWM inverter is currently being built.

**DC-DC Converter**

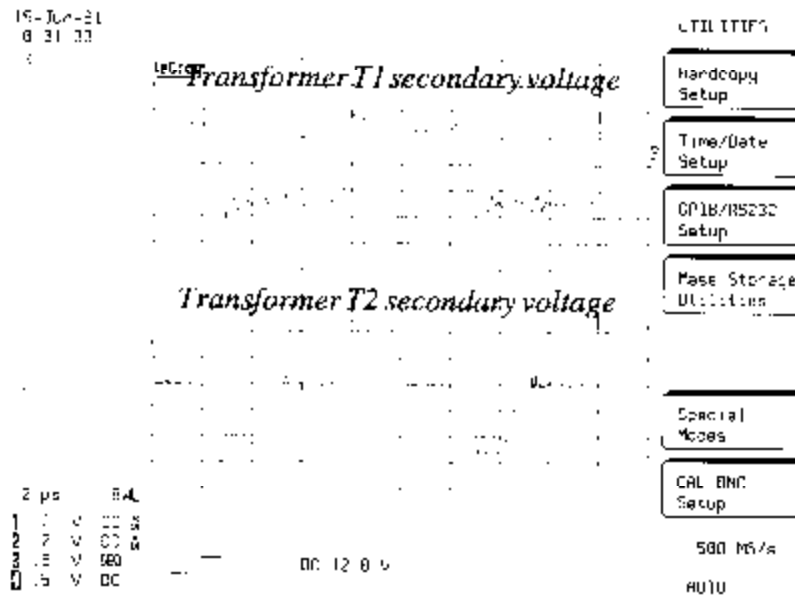
Fig. 7.1 shows the DC-DC converter setup currently under development. The PC board includes the complete power stage of the DC-DC converter and the UC3875 ICs required to give gate pulses to the switches. The converter also includes a 20W flyback converter which provides the control power for the entire system.



**Fig. 7.1. 1.5kW Prototype of the DC-DC Converter**

Results obtained for the DC-DC Converter

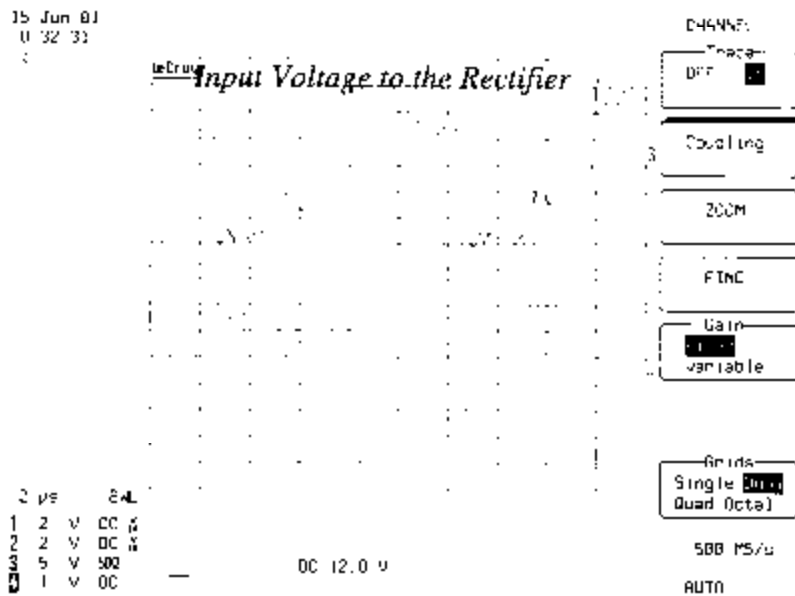
Fig. 7.2 shows the transformer secondary voltages. The waveforms match the idealized



**Fig. 7.2. Transformer Secondary Voltages**

waveforms shown in Fig. 2.3.

Fig. 7.3 shows the addition of the two transformer voltages to form the stepped voltage



**Fig. 7.3. Input Voltage to the Diode Bridge Rectifier**

waveform, which would be rectified by the full bridge diode rectifier.

Fig. 7.4 shows the voltage after rectification. As it can be seen, the switching frequency ripple in the voltage is very small. Thus, the output filter required to smooth this DC voltage would be greatly reduced as compared to the conventional PMC.

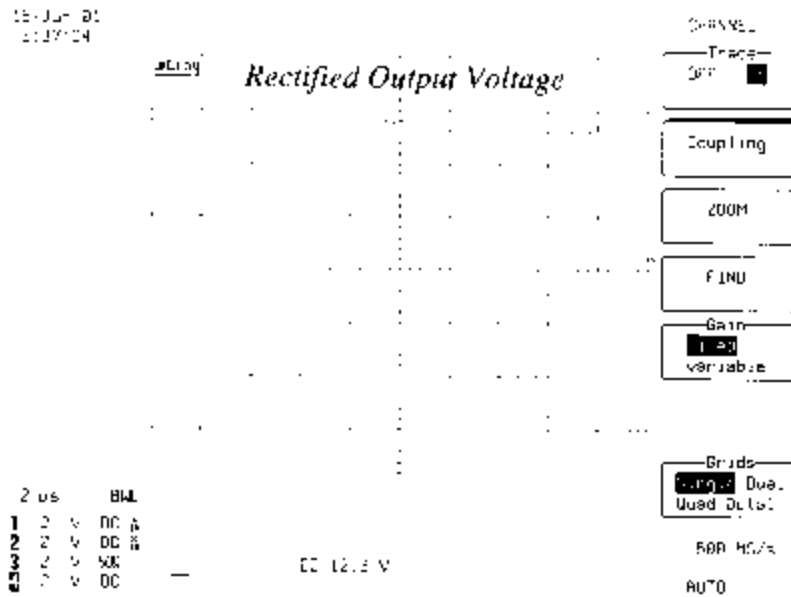


Fig. 7.4. Rectified Output Voltage

The ZVS characteristics of the three legs of the converter, at no load, are shown in Fig. 7.5. All three legs are found to have zero voltage turn on at no load.



Fig. 7.5. ZVS characteristics at no load

### **Timeline for the Project**

The following timeline has been decided upon in order to complete the hardware prototype by August.

June 17 - June 23 : Complete the testing of the DC-DC converter

June 17 - July 7 : Complete the assembly and testing of the PWM inverter

June 23 - July 7 : Complete the assembly of the controller PCB

July 7 - July 30 : Test the interconnected system with their controllers for different types of loads.

### CONCLUSIONS

The proposed topology is found to be ideally suited for converting the low voltage DC to the required 60Hz AC. The novel DC-DC converter topology used to step up the DC voltage enables zero voltage switching for all the controlled switches in the topology upto 10% load without significant conduction loss penalty. There is also a substantial decrease in the input and output filter requirements for the converter. The two winding transformers prevent the midpoint of the DC link from floating. The transformers also help to maintain the voltages at the capacitors inspite of load imbalances.

The use of two half-bridge inverters to achieve the split single phase output enables DC to AC conversion with minimum number of switches. The half bridge inverter also ensures a balanced load on the two halves of the DC link even under extreme load imbalance.

The use of the DC link capacitor to store the difference between the input and output energies ensures that a near constant DC current is drawn from the fuel cell, maximizing its efficiency and life.

The control of the system is also extremely simple, with the DC-DC converter and the PWM inverter having independent control loops, minimizing interactions between the control loops of the two systems.

## REFERENCES

- [1] Friedman, Richard, "What the Future Holds for Utilities and Distributed Generation," *Utility Automation*, vol. 4.9, November 1999.
- [2] Boegli, U. and Ulmi, R., "Realization of a New Inverter Circuit for Direct Photovoltaic Energy Feedback into the Public Grid," *IEEE Transactions on Industry Applications*, vol. IA-22, no.2, March-April 1986, pp.255-8.
- [3] O'Sullivan, George. A. "Fuel Cell Inverters for Utility Applications," *Proc. Power Electronics Specialists Conference (PESC'00)*, 2000, pp. 1191-94.
- [4] Nonaka, S. and Harada, K., "Utility Interactive PV System used The Single-Phase Composite PWM Voltage Source Inverter," *Proc. International Power Electronics Conference*, 2000, pp. 176-180.
- [5] J.A.Sabate, V.Vlatkovic, R.B.Ridley, F.C.Lee and B.H.Cho, "Design Considerations for High-Voltage Full-Bridge Zero-Voltage-Switched PWM Converter," *Proc. IEEE Applied Power Electronics Conference*, 1990, pp.257-284.
- [6] R.Ayyanar and N.Mohan, "Full-Load-Range-ZVS Hybrid DC-DC Converter with Two Full-Bridges for high-Power Battery Charging," *Proc. International Telecommunications Energy Conference (INTELEC'99)*, 1999, pp. 20-2.
- [7] R.Ayyanar and N.Mohan, "An Improved Full-ZVS-Range Hybrid DC-DC Converter with Low Filter Requirement Capable of Adding and Subtracting the Controlled and Uncontrolled Sections," *Proc. Power Electronics Specialists Conference (PESC'00)*, 2000, pp. 179-184.
- [8] D.Venable, "The K Factor: A New Mathematical Tool for Stability Analysis and Synthesis", *Proceedings Powecon 10*, 1983.
- [9] SABER Manual, Analogy Inc., 1999.

**You have reached the end  
of this final report.**

**Use the button below to  
return to the Main Document**