

Golden, June 5th 2001

Robert Myers
799 North Beverly Glen
Los Angeles, CA 90077

Bob:

I am enclosing the report for the 2001 Future Energy Challenge prepared by the undergraduate team of Colorado School of Mines.

Unfortunately, the team was not mature enough to endure all adversities for such competition. They graduated in May, got very good jobs, and due their new professional involvements they did not want the commitment to work on the final prototype to send for evaluation. Our school is small and only by next academic year we could assemble a new team to finish this project.

Despite the fact that it was not achieved a working prototype, I have the personal feeling that it was very exciting to advise this team. They started from knowing nothing about power electronics to eventually learn a lot of important and contemporary power electronic issues.

I wish all the success with the other teams involved in the competition.

With my best regards,



Marcelo Godoy Simoes



Memo

To: 2001 Future Energy Challenge: Report Judging Board
From: Colorado School of Mines, 2001 Future Energy Challenge Team
Date: June/1/2001
Re: Final Report for the 2001 Future Energy Challenge Project

This letter is being written by the members of the Colorado School of Mines, 2001 Future Energy Challenge Team, in regards to the current team report that has been transmitted. This report contains all current information and research on the Fuel Cell Inverter project that the team has come up with since the formation of the project in August.

Within this document, the Fuel Cell Inverter Team has enclosed an executive summary of the Fuel Cell Inverter report, which discusses the main requirements of the project as well as the general approach that the Fuel Cell team has used to accomplish the project goals. In order to gain a detailed knowledge of the project, the team has also enclosed a detailed report, which includes the background of the Fuel Cell, Design Specifications of the Fuel Cell Inverter, the Design Concept, Project Funding and Budgeting, Simulation Results, and the final cost analysis. Appendices have also been added to the end of this proposal, which give the Fourier analysis of the fuel cell inverter, and a summary of the cost analysis.

Although much progress has been made in regards to the 2001 Future Energy Challenge Project, the team at the Colorado School of Mines (CSM) has been unable to finish the prototyping of the fuel cell inverter. Also, due to lack of sufficient team members available during the summer, the CSM team will not be able to continue the 2001 Future Energy Challenge project for competition purposes. Therefore, in order to finish this endeavor, the CSM team has decided to pass on the 2001 Future Energy Challenge project to next year's senior design students. The current team hopes that by effectively recruiting and teaching potential students about the progress made on the current fuel cell inverter, that the project will be finished sometime during the next academic school year.

The 2001 Future Energy Challenge Team has enjoyed the challenge of designing, simulating, and prototyping the fuel cell inverter. If you have any further questions or comments on the 2001 Future Energy Challenge project, please feel free to contact team members through the Colorado School of Mines EG Division or by emailing the team leader at jseverso@mines.edu. Thank you.

Kary Wain

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Dan Adams

Enc.

Colorado School of Mines Engineering Division

FUEL CELL INVERTER TEAM

Final Report

Submitted to

2001 Future Energy Challenge: Report Judging Board

by

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May 1, 2001

TABLE OF CONTENTS

TITLE PAGE 1
TABLE OF CONTENTS & APPENDICES 2
LIST OF FIGURES & TABLES 3
I. INTRODUCTION. 4
Fuel Cell Background	
Goals of 2001 Future Energy Challenge	
II. DESIGN THEORY 5
Methods for Reducing Inverter Cost	
Implementation of our Design	
III. SIMULATION ANALYSIS 8
Pspice Simulation	
IV. PROTOTYPE SPECIFICATION.	13
Power Electronics Components	
V. EXPERIMENTAL RESULTS.	20
Testing of 1.5kW Prototype	
VI. COST STUDY.	21
Market Analysis of Projected 10kW Inverter	
VII. EVALUATION OF RESULTS.	22
Societal Impact of Design and its Future	
VIII. BIBLIOGRAPHY	23

APPENDICES

APPENDIX A	24
APPENDIX B	25
APPENDIX C	26
APPENDIX D (GLOSSARY OF TERMS)	27

LIST OF FIGURES / TABLES

FIGURE 1: BLOCK DIAGRAM OF OUR INVERTER DESIGN	6
FIGURE 2: SCHEMATIC OF INVERTER SYSTEM	8
FIGURE 3: SCHEMATIC OF SCR MODEL	9
FIGURE 4: SCHEMATIC OF CONTROL SYSTEM	10
FIGURE 5: OUTPUT FROM WAVEFORM CONDITIONING	11
FIGURE 6: DENSITY MODULATION OF PULSES	12
FIGURE 7: FUNCTIONAL SCHEMATIC OF INVERTER	16
FIGURE 8: SCHEMATIC OF BATTERY BUFFER SYSTEM	18

I. INTRODUCTION

FUEL CELL BACKGROUND

Fuel cells convert chemical energy to electrical energy by reversing the electrolysis process, an idea first conceptualized by Sir William Grove in 1839. When hydrogen is passed through an electrolyte to combine with oxygen, free electrons are produced and diverted through an electrical circuit and corresponding load, leaving behind byproducts of water and heat. As a result, the fuel cell is attractive due to its combination of being environmentally friendly and having a relatively high efficiency. Although many in the power industry expect fuel cells to soon replace conventional fossil fuel power generation, the cost of fuel cell systems continues to hold back a wide spread revolution of fuel cell use in residential and commercial applications. Practical fuel cell systems today consist of the fuel cell itself, control systems, a fuel reformer to extract hydrogen from fossil fuels such as methane or natural gas, and an inverter to convert the final output from DC to an AC power that can be readily used in residential and commercial applications.

GOALS FOR 2001 FUTURE ENERGY CHALLENGE

The 2001 Future Energy Challenge, sponsored by the US Departments of Energy and Defense, among others, aims to help reduce the cost of the fuel cell system in order to spark a residential interest in the fuel cell. While the cost of the fuel cell subsystem has been coming down for years as a result of research, the inverter now takes up one third of the total system cost. By reducing the cost of the inverter to \$500 for a 10kW inverter, it is expected that the fuel cell will present an economical alternative to other sources of electricity. It is hoped that tapping into collegiate innovation in this area will lead to the cost revolution necessary to spark the fuel cell's

widespread residential use. College teams are asked to build a split-single phase 120V, 60Hz, 1.5kW prototype for testing purposes to demonstrate the strength of their design. In return, sponsors have donated a \$50,000 prize to be awarded to the team that best meets this cost target while maintaining minimum requirements in terms of efficiency, size and weight, and remaining acceptable in the areas of performance, reliability and safety.

II. DESIGN THEORY

METHODS FOR REDUCING INVERTER COST

After reviewing the aggressive cost target and accompanying specifications for the project, we decided that an un-conventional design was necessary for success. While the standard pulse width modulation (PWM) designs on the market today achieve a good result in terms of power quality, they are expensive. Following are the methods that we chose with the hope of reducing the inverter cost while maintaining minimum performance standards:

- 1) By using less expensive switching devices known as silicon controlled rectifiers (SCR's) instead of modern power MOSFET's or IGBT's, we could bring the cost of the power electronics down. We did not believe that making minor changes from conventional design would enable us to reach our cost target. In order to use SCR's in a stand-alone system, we decided on a series resonant converter design to provide a zero-crossing current for turning the SCR's off.
- 2) This also takes advantage of soft-switching the SCR's since there is no power loss as a result of turning off our switch. As a result, we expected that the heatsink and packaging requirements would decrease, and reduce our cost.

- 3) By taking advantage of the automatic turn-off aspect of the SCR's, we planned to use a simpler analog control system than comparable digital control systems.
- 4) By switching our SCR's at 20kHz we could take advantage of a smaller high frequency transformer to step up our voltage to the final 120V.

IMPLEMENTATION OF OUR DESIGN

In order to use our SCR's in our system, we had to create a current that passes through zero. Once SCR's are turned on, they remain on until either the current through the SCR stops, or is diverted through another path. By using a resonant converter, the second-order nature of the circuit allows a sinusoidal current to pass through the circuit. As the current begins to swing negative, the SCR's turn off and wait for another signal to turn on. The negative current is diverted through an anti-parallel diode across the SCR in order to tank the energy stored in the LC components.

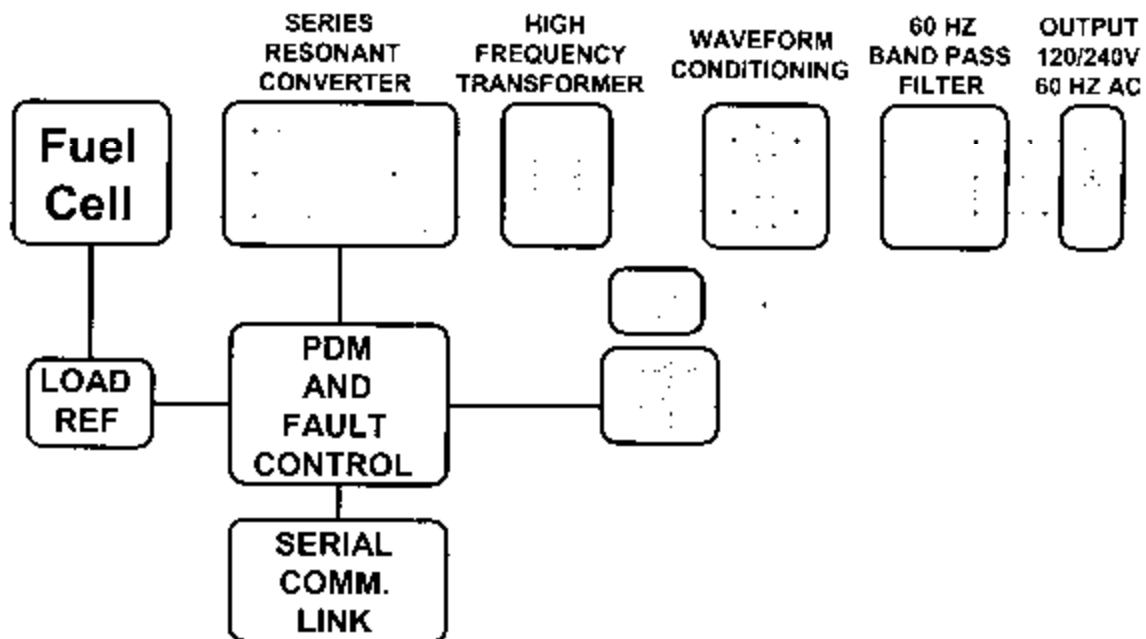


FIGURE 1: BLOCK DIAGRAM OF OUR INVERTER DESIGN

While a half-bridge resonant converter using only two SCR's could be used, the full-bridge configuration is needed for higher power levels. If the initial prototype were to give good results, a half-bridge design could be considered to further reduce our cost.

The series resonant topology is implemented by using the primary reactance of the transformer as the inductance in the resonant converter. This reduces the number of components in the system and transfers our power to the load. The transformer is known as a high frequency transformer, in that it is designed to transfer higher frequency of power. The size of a transformer is inversely proportional to its frequency, based on its magnetic characteristics, allowing us to reduce the size and cost of our transformer as we increase the frequency of our circuit. The transformer is also needed to step-up our voltage from the nominal fuel cell voltage of 48V to the 120VRMS output. If a 60Hz transformer were used at the final stage of our topology, its size and cost alone would endanger the project goals. A split-single phase output can be generated by pulling two separate windings off the transformer core. By switching the polarity of the windings, the two outputs are 180 degrees out of phase, and together produce a 240VRMS output.

From our control circuit, the SCRs are pulse density modulated around 60Hz to create a pulsed waveform with varying density coming from the transformer. In order to create the positive and negative phases of our sinusoidal output, we had to insert an intermediary "waveform conditioning" or matrix converter phase to control the sign of the resulting waveform. By reversing the allowed flow of current, the positive and negative phases alternate between the split outputs. Adding a 60Hz low pass filter at the end extracts the 60Hz component from the pulsed waveform passed from the fuel cell.

III. SIMULATION ANALYSIS

To design and test the control systems we used an array of simulation software. The primary software used was P-Spice by Orcad. This software allowed us to model the power electronics, transformer and filter. While these systems were not completely accurate with the models used, they did work well for controller design. The schematic that was used to represent the entire system is located below.

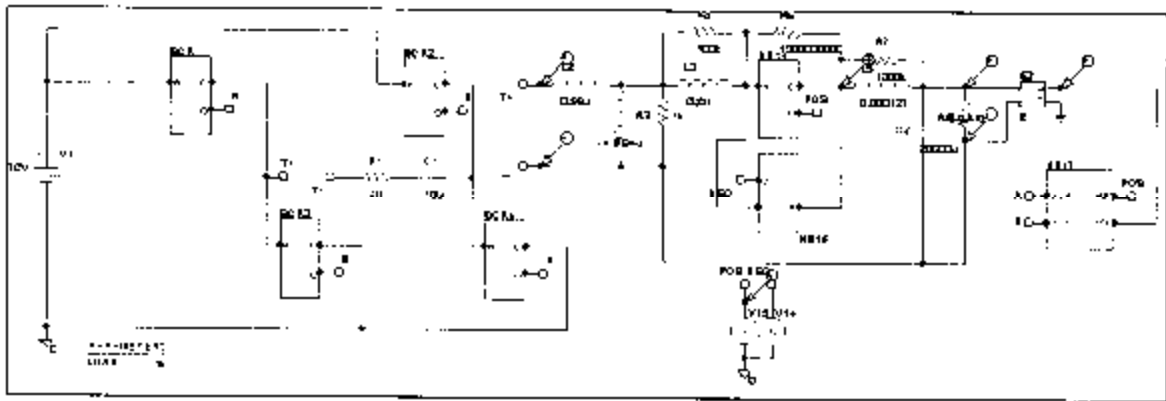


FIGURE 2: SCHEMATIC OF INVERTER SYSTEM

The system has five main model points. On the left most side we have a 70V DC source simulating our fuel cell. Just to the right of that there are four blocks that represent the SCR's and the resonant converter. This is where the 20kHz pulses are created. The inductance for the converter is found in the transformer windings, the next part of the model. It is modeled as a T-model transformer. Connected to it we have another two SCR blocks that represent the matrix converter. After the matrix converter we see the 60Hz filter and the load. Attached to the load is the control system.

The SCR's are modeled with the schematic below. This model was used to minimize the number of components that were needed for the schematic and kept us in the evaluation/student version of P-Spice. This model has the same general function as

the real SCR's will it does not have a switching limit, or much transient changes like our SCR's will. These factors cannot be modeled well with any simulation though and will be best determined with tests rather than simulation.

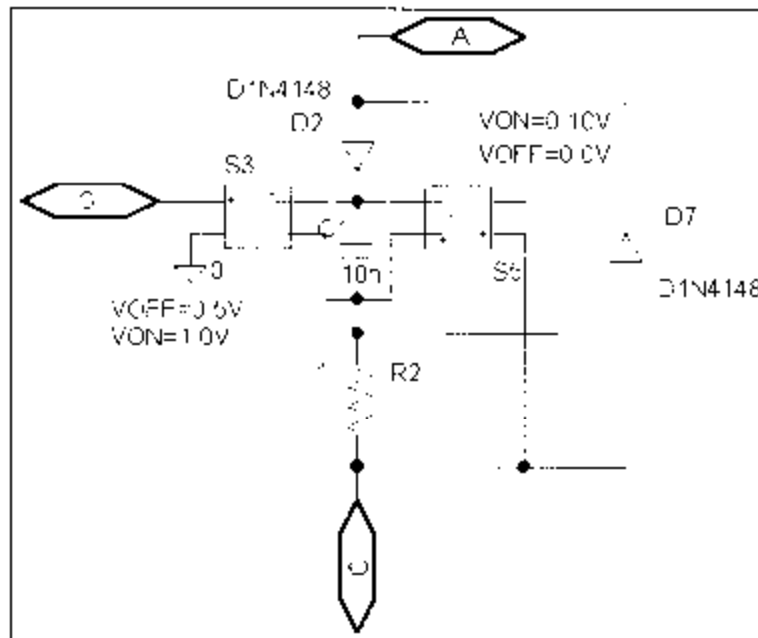


FIGURE 3: SCHEMATIC OF SCR MODEL

The model uses two switches to determine if the SCR should be on or not. One switch acts as the systems gate. When the node labeled G receives a voltage greater than 1 volt it turns on and allows current to travel forward. The diode makes sure that current does not flow in the reverse path. The small resistor and other switch make allow the current to continue to flow as long as there is a positive current. This is done by controlling the switch with the voltage across the resistor. The diode on the right is used to allow a reverse current path, similar to our SCR's.

This model was used for both the matrix converter and the resonant converter. The only difference is that the matrix converter does not have anti-parallel diode. This

model worked well for each only because hand calculations were used to verify that we were not exceeding the switching limitations of the SCR's in the simulation.

The controller that we decided to use took advantage of the nature of the error signal and dynamics of the system. This controller compares the output voltage to a reference voltage. If the error is larger than the range allowed it allows the timed pulses to pass to the gate drives. The timed pulses are generated with the width of half of the maximum frequency and a delay between the pulses that makes the total width of each pulse correspond to the minimum frequency of the resonant converter. These frequency changes happen because of the different loading on the transformer thus changing the impedance of the transformer. The schematic that was used to test the system is located below.

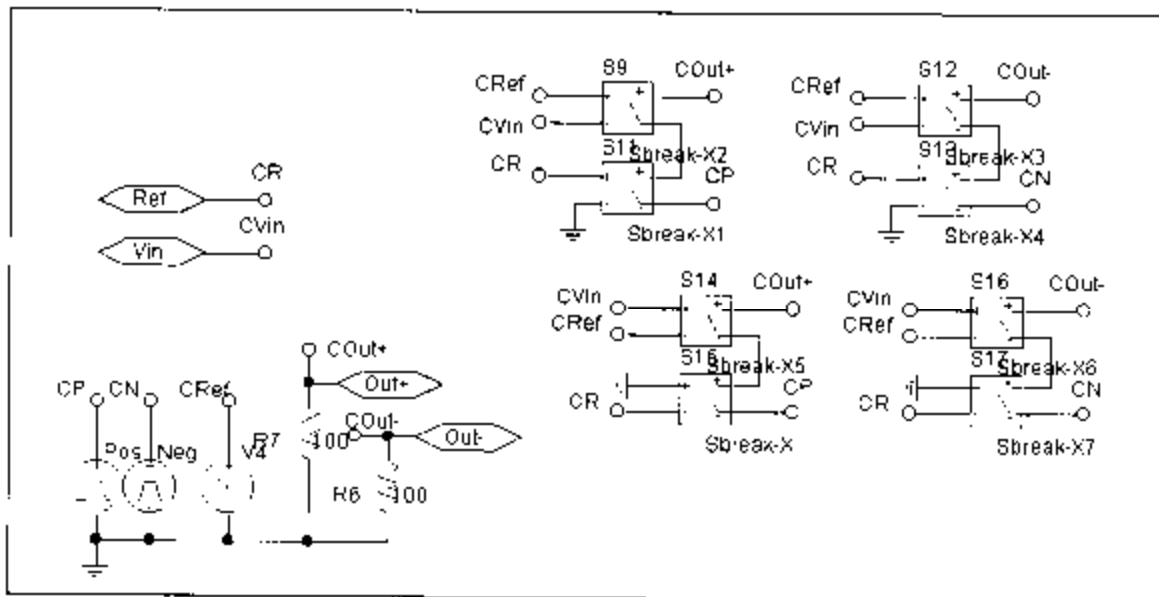


FIGURE 4: SCHEMATIC OF CONTROL SYSTEM

To implement this system we will be using an array of analog and digital devices. A op-amp is used to create a hysteresis amplifier that will determine if the error is too great. The output of this will be a CMOS compatible signal that will pass through two op-

amps, one checking for phase of the output and the other checking if a positive pulse is desired. The final output of the AND gates will be passed through an XOR gate assuring that a pulse in the opposite direction has not been commanded at the same time. While this is not possible in the ideal situation, if this were to happen some how, the system would short and break. This needs to be protected against.

From the simulation we were able to create the following graphs that support our original planned system. This includes pulses that are almost four times the input DC voltage peak to peak across the input of the transformer. A error signal that has a varying frequency from low to high back to low for each half cycle. We also see that the current is always positive through the positive part of the wave and negative through the negative section. These all conclude that our system will work. There are many small differences in these models that will not make the simulation exactly match the actual output but the differences will be minimal. We are also planning for these differences.

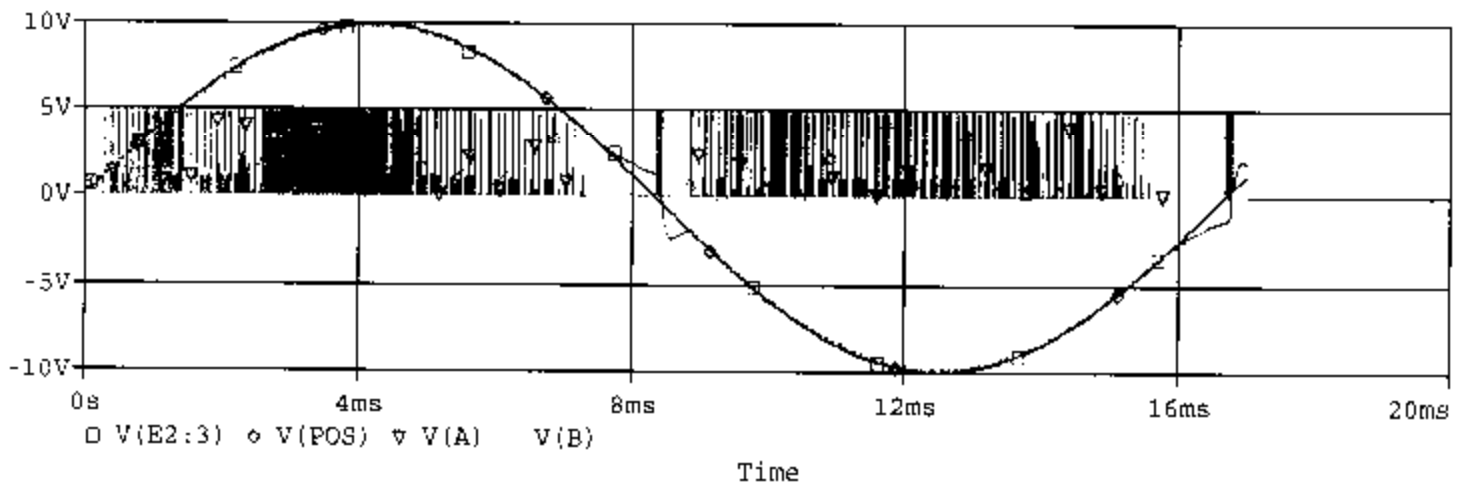


FIGURE 5: OUTPUT FROM WAVEFORM CONDITIONING

The graph above shows the output voltage on top of the reverse voltage. It is important to note that the output of the system will not be 10V peak to peak but 120V

RMS, for the controller a reference signal that in this model is 10V peak to peak is used for control.

Also on the same graph the signals that are sent to the gate drives of the SCR's are places. It is easy to notice that this is pulse density modulation because while the size of each command pulse is the same they become more frequent in the middle of the half cycle. Each of the command pulses corresponds to an actual pulse that is created by resonant converter. A graph of a series of these pulses is shown below.

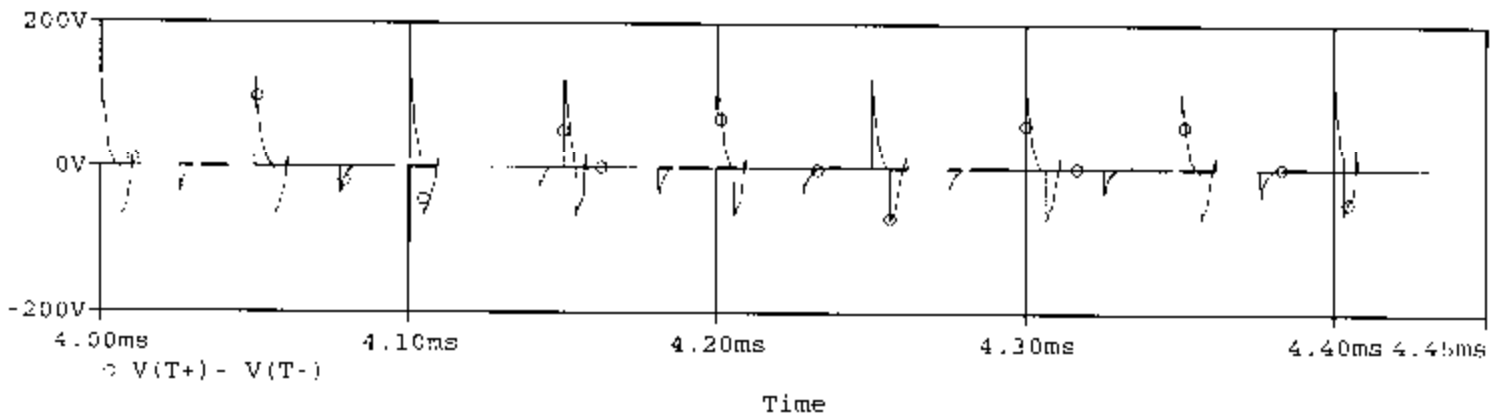


FIGURE 6: DENSITY MODULATION OF PULSES

Each of the pulses was created by one small gate signal. The pulse has an amplitude of almost twice the input voltage and a pulse width corresponding to 20kHz. This also shows the spacing between pulses that is allowed so that the pulses do not overrun each other and short the system.

This simulation has provided many key data points for our group that will reassure us when we test the system that our output is correct and give us a better perspective of what to expect from our system. While many of the models that were used simplified logic, the end results are close to what our system will actually do.

IV. PROTOTYPE SPECIFICATION

RESONANT CONVERTER SCRS

In order to achieve the best resolution in our pulse density modulation, we need to use the fastest switching frequency that our circuit will allow. A faster switching frequency means that we have more opportunities to send pulses and can therefore increase the resolution of the 60 Hz waveform. However, initial fourier analysis, as presented later in this report, seems to indicate that our output voltage varies little with a change in switching frequency, since most of the waveform is passed at higher frequencies. Nevertheless, a higher switching frequency will reduce the size and cost of our transformer and resonant components. Unfortunately, SCR's are not generally used at high frequencies, and a lot of work was spent in finding a module that could work with our design.

The switching frequency of an SCR is limited by its turn-off time, t_q , which is the minimum time that the device needs to rest before it can pass another pulse safely. Common SCR's used for high power ratings with slower switching requirements have a turn-off time on the order of $t_q = 100\mu\text{s}$, and cost only a few dollars per device. However, in order to switch at 20kHz, we needed a turn-off time on the order of $t_q = 10\mu\text{s}$. International Rectifier carries inverter SCR's with turn-off times ranging from $t_q = 10\mu\text{s}$ to $20\mu\text{s}$, but this would still be cutting our design close. Finally, Dynex Semiconductor, a relatively unknown company, was found to carry an asymmetrical SCR with a maximum turn-off time of $t_q = 6\mu\text{s}$. An asymmetrical SCR includes a built-in anti-parallel diode across the SCR, which is what our design required. The frequency of these devices can also be increased by using reverse-gate bias control of the SCRs [1]. This amounts to

applying a negative voltage to the SCR gate when we want to turn off the device so that it is forced into turning off faster. For this ASCR that we are using, it is reported that turn-off times of $t_q = 2.5\mu\text{s}$ can be achieved using reverse-gate bias, which could allow a switching frequency of at least 50kHz. However, due to the complexity of the SCR's gate drive circuitry, we decided to prepare the initial prototype to switch at 20kHz, and decide after testing if a higher frequency should be considered. The datasheet for our resonant converter SCR is shown in Appendix A, Section 1. A big blow to the project came when we received a price quote of \$67.00 for each device. With four of these in our full-bridge design, more than half of our 10kW budget would be taken up in the 1.5kW resonant converter SCR's. Nevertheless, we decided to continue with our design, and determine later if other SCR's should be used or if the price could come down when produced on a widespread basis.

Another major task relating to the resonant converter SCR's involved coming up with a gate drive circuit to fire the SCR's. We found that unlike modern devices such as MOSFET's or IGBT's, general gate drives are not marketed for SCR's, so we had to make our own from scratch. After more than a month of testing and revision, the gate drive circuit presented in Appendix A, Section 2 was found to achieve specific control of the ASCR with a 5V control signal. The gate drives are isolated from the control circuit using a Semikron pulse transformer, allowing a relative gate signal at any voltage.

HIGH FREQUENCY TRANSFORMER

Our inverter topology uses a high frequency (HF) transformer to pass the voltage pulses from the resonant converter to the load. The frequency rating of the transformer

can be determined as the minimum signal frequency being sent through the transformer, since the lowest frequency will cause the most transformer heating. We are using the primary impedance of the transformer as our resonant inductance, saving money and space instead of buying another inductor for the converter. This type of series configuration of the converter is called a series resonant converter. It was initially thought that we could purchase an off-the-shelf transformer to use in our design, but this was found to be unlikely due to the specialized requirements that our model would require. Some time was spent investigating transformer design [2], but an industrial model was donated to the team before this was pursued too heavily. The transformer that we have is rated at 20kHz for a 2kW load, and can be used to test our initial prototype, but is not specific enough to our design to fulfill final requirements. Custom design and construction of a transformer is expected to be about \$1000.00, which is more than our current budget can sustain. In addition, we are not certain about what turns-ratio is needed to produce a waveform large enough to extract 120VRMS. It would not be economical to find out that the determined turns-ratio was wrong after spending such a large amount to construct it. Figure 7 shows the overall functional schematic of our proposed inverter, including the split single-phase outputs coming off the transformer. The transformer will be a 3 winding, dual center-tap 20kHz transformer, with various possibilities as to core type and configuration, and a turns-ratio of at least 4 to 1. However, it will not be practical to build a transformer until initial testing is completed along with simulation demonstrating the ideal transformer specs.

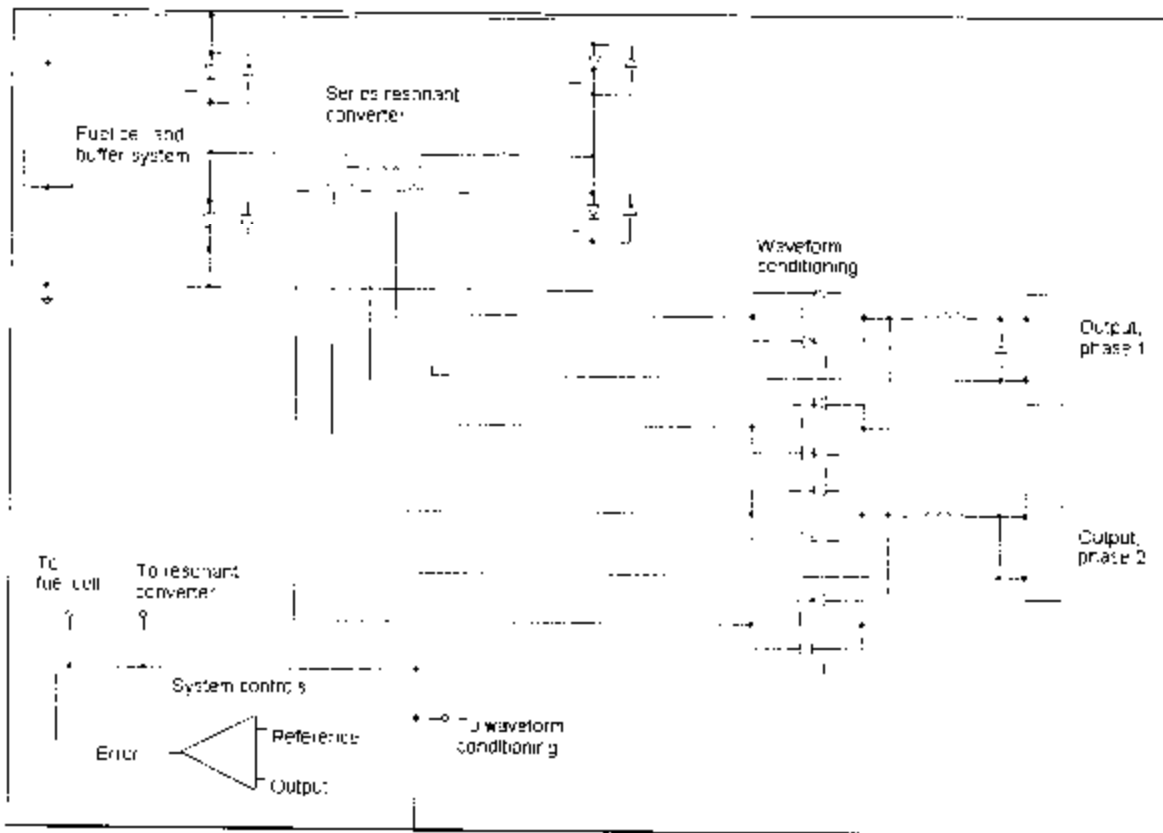


FIGURE 7: FUNCTIONAL SCHEMATIC OF INVERTER

RESONANT CONVERTER CAPACITOR

The resonant converter capacitor serves along with the primary impedance of the transformer to create the sinusoidal current necessary for turning off the resonant SCR's. The resonant frequency of the LC circuit is determined by the switching frequency of the SCR's, in order to create current pulses with the appropriate width. One problem with these capacitors is that they need to be non-polar capacitors since their polarity reverses with the operation of the circuit.

WAVEFORM CONDITIONING SCRS

The waveform conditioning SCR's are different from the resonant converter SCR's in that they do not modulate the output signal, and therefore switch at a much lower frequency of 60Hz. The purpose of these SCR's is to force the polarity of the output to switch at 60Hz. The resonant converter is intended to pass both positive and negative pulses the whole time, while being density modulated based on the phase of the signal. During the positive phase of the 60Hz waveform, the waveform conditioning phase will allow the positive pulses to pass to the primary output signal, while the negative pulses are passed to the secondary reverse-polarity output. During the negative phase of the 60Hz waveform, this operation is reversed, allowing both polarities to pass through to both outputs. The SCR's do need to be able to block the voltage of the reverse-polarity pulses, which will be determined by the turns-ratio of the transformer. For the initial prototype, the 2N6507 model SCR was selected based on its 25A, 400VDRM rating. However, if the transformer turns-ratio is increased, an SCR with a higher reverse voltage blocking rating may be required.

LOW PASS FILTER INDUCTOR AND CAPACITOR

The low pass filter is designed to pass the 60Hz component of our waveform while absorbing the higher frequencies on the order of our switching frequency. This depends heavily on the controller to keep the system stable and producing a good modulation around 60Hz. Fourier analysis of our expected open loop waveform, as seen before the low pass filter, is shown in Appendix B, Sections 1 & 2. Although our actual feedback controlled waveform will be slightly different as it responds to the system, the

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open loop signal gives a lot of insight into how the system will operate. As mentioned earlier, the first harmonic of the waveform, or the 60Hz component, has a magnitude of about a third of the peak of our modulated pulses. This seems to indicate that we will need 510V peaks in order to produce a peak 120VRMS waveform. Once again, testing and further simulation will determine if this is necessary. If it is, we may need a turns ratio of 10 to 1, which could effect the rest of our design. Analysis also indicates that most of the harmonic ripple does occur at higher than frequencies 50 times the fundamental frequency of 60Hz, indicating that almost any low pass filter should be able to cut off these components reasonably well. The fourier analysis can easily be updated to reflect changes in switching frequency or modulation period for more accurate results.

BATTERY BACKUP SYSTEM

Due to the long transient time of the fuel cell, and the near instantaneous rate that loads can be applied, it is necessary to provide a buffering system to take up the load until the fuel cell has reached the new required output level. The buffering system also needs to be able to prevent damaging back current from reaching the fuel cell. In addition to these two functions, the system will have to maintain a charge on the batteries.

To make up for voltage drops in the fuel cell source, when a load is increased, diode D4 will turn on. This prevents the voltage entering the inverter from dropping below the voltage level of the batteries. Diode D3 prevents current from flowing backwards through the fuel cell. The LM324 op-amp is used to compare the voltage level of the battery to a reference voltage. This is to determine the charge on the battery.

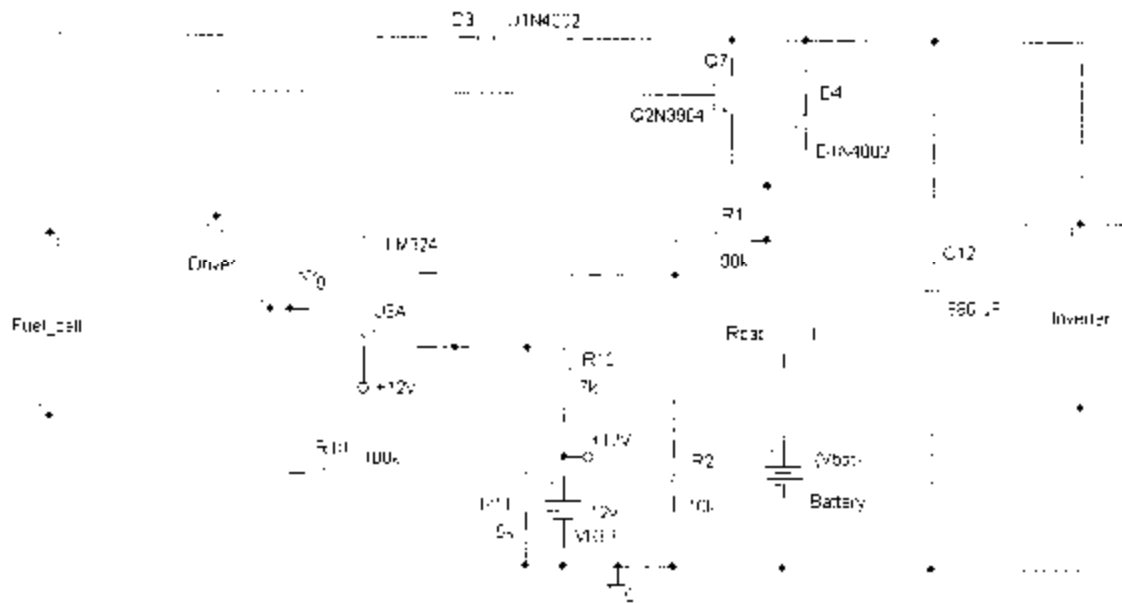


FIGURE 8: SCHEMATIC OF BATTERY BUFFER SYSTEM

Using 4 12-volt batteries, the full charge output voltage will be 50.8 volts. The op-amp system will turn on Q7 when the battery voltage drops below 50 volts (corresponding to approximately 84% of full charge). This allows current to flow from the fuel cell into the batteries, charging them. Through the use of the positive feedback, Q7 will not turn off until the batteries are fully charged. Simulation of the battery backup system from Figure 8 is presented in Appendix B, Section 3.

The operation of the inverter will produce pulses of current that travel in the opposite direction of the normal direction of the current. Diode D3 protects the fuel cell from this reverse current. When the battery is fully charged, and Q7 is turned off, this reverse current travels into capacitor C11, and is returned to the inverter. When Q7 is turned on, the current will flow into the battery, helping to charge it.

V. EXPERIMENTAL RESULTS

At this point in the project, we have very little in the area of experimental results. We do have intermediary results with respect to our SCRs and gate drives, but not from our actual prototype. As indicated earlier, we have developed a specialized isolated gate drive for our high power SCRs. Using this circuit, we can turn on an SCR at specified intervals with a +5V control signal. In addition, due to the isolation achieved by the pulse transformer in the gate drive, the SCR can be turned regardless of its cathode voltage. We have tested the SCR circuit with a 120V sinusoidal input with 40W light bulb load. Using a function generator for control, we can blink the light on and off at a controlled rate. The gate drives also work to turn on the low-power SCRs used in the matrix converter. However, the gate drive produces more than enough current, so a 2k Ω resistor is used in series with the gate signal, in order to protect the SCR. We have succeeded in ordering most of our parts for an initial prototype, but have not completed its construction. Testing of the prototype should be done in stages, instead of putting it all together and turning a switch on. At this point, we are ready to test the resonant converter with a load, but even this would take a lot of preparation. After the resonant converter is tested, the next phase would be to add the matrix converter, and finally the low pass filter. However, with this initial prototype, we cannot test it at full load, or expect a peak of 120VRMS at the output, due to the equipment and components that are available. Our transformer has a step up ratio of 4:1, but some of our analysis is suggesting that it should be a lot higher to produce enough voltage to extract a 120VRMS signal with the low pass filter.

VI. COST STUDY

Appendix C contains our cost analysis datasheets for both the money spent on our 1.5kW prototype and an estimated market manufacturing cost of the prototype on a 10kW level. For Senior Design, extra components, such as our SCR's, were ordered in case some are destroyed during testing. Actual money spent from our Senior Design budget comes to about \$1000.00 for components and an additional \$200.00 for printing and other miscellaneous costs. Appendix C, Section 1 is the itemization of the costs and quantities ordered of the major components of our system, coming to \$936.62. Money was also spent on minor allotments, some of which were abandoned, bringing an estimate of \$1000.00 spent by the team on initial construction of our prototype. Appendix C, Section 2 contains an estimated prototype cost under mass production when scaled to 10kW. These numbers are not definite, especially since testing of our 1.5kW prototype is not complete, and only reflect what market conditions will have on the cost of our projected inverter. Our basic design consists of the following sub-circuits: a full bridge inverter circuit constructed from SCR devices, a resonant inverter circuit containing 5 capacitors, a high frequency transformer (inductance to be used in the resonant circuit), 2 full-bridge waveform conditioning circuits containing a total of 8 SCR devices, a control system, and a low-pass-filter circuits containing a total of 4 inductors and 2 capacitors. While some of our actual components may change when scaling to 10kW, the number of sub-systems should not change.

VII. EVALUATION OF RESULTS

Our inverter design has the potential to revolutionize both the alternative energy and inverter markets, based on the expected performance of our design topology. However, until initial testing has been completed, we cannot say one way or another as to the effect of our inverter on society. While some on our team consider our simulation to be complete, we still do not have a clear picture from simulation indicating that the system is operating as we expect. Furthermore, fourier analysis of our open loop waveform brings up more questions that can only truly be answered through experimental testing. As a team, we have made good progress on a revolutionary concept, given our lack of background in the power electronics field, but more work must be done before the strength of our concept can be evaluated. As for the inverter itself, if costs even approached levels such as \$50/kW, it would have a big impact on industry. Currently, we do believe that if we can make our system work, it will bring the inverter cost down from current levels.

Fuel cells are continuing to gain recognition in industry as an environmentally friendly alternative energy source with potential applications in both industry and residential homes. Whether or not they are used for their price and efficiency or for self-protection from uncertain power resources, fuel cells seem to be the wave of the future. With this in mind, a complete fuel cell system will be needed that can operate together as a unit. We do believe that control of the fuel cell system should come from the inverter, as proposed in this project, in order to maximize performance, efficiency and safety, while minimizing the cost of fuel cell system in residential applications. Now, all that remains is to convince the residential consumer to invest in the fuel cell dream of the future.

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APPENDIX A : RESONANT CONVERTER DATASHEETS

- I. RESONANT CONVERTER DATASHEET
- II. SCR GATE DRIVE CIRCUIT

APPLICATIONS

- High Frequency Applications
- Regulated Power Supplies
- Capacitor Discharge
- Ultrasonic Generators
- Induction Heating

KEY PARAMETERS

V_{DRM}	1600V
$I_{T(AV)}$	44A
I_{TSM}	550A
dV/dt^*	600V/ μ s
di/dt	2000A/ μ s
t_a	6.0 μ s

* dV/dt Available to 1000V/ μ s

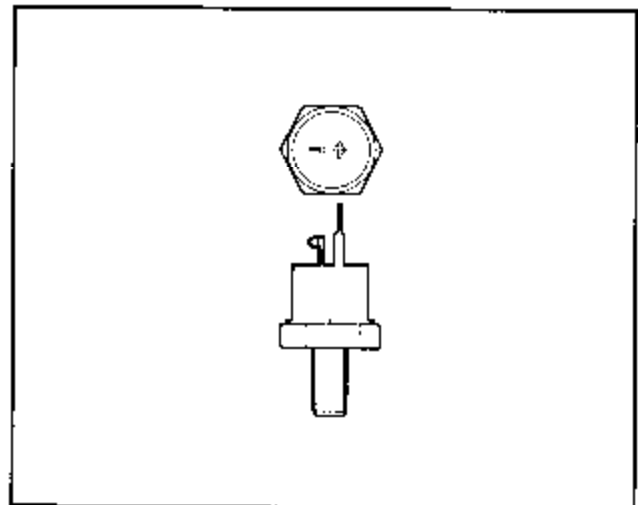
FEATURES

- The ACR44U is a glass passivated asymmetric thyristor which has exceptionally fast turn-off capabilities combined with good turn-on characteristics.

VOLTAGE RATINGS

Type Number	Repetitive Peak Off-state Voltage	Repetitive Peak Reverse Voltage
	V_{DRM} V	V_{RRM} V
ACR44U 16LE	1600	2
ACR44U 14LE	1400	2
ACR44U 12LE	1200	2
ACR44U 10LE	1000	2
ACR44U 08LE	800	2

Lower voltage grades available.



Outline type code: SO28.
See Package Details for further information.

CURRENT RATINGS

Symbol	Parameter	Conditions	Max.	Units
$I_{T(AV)}$	Mean on-state current	Half wave resistive load, $T_{case} = 80^{\circ}\text{C}$	44	A
$I_{T(RMS)}$	RMS value	$T_{case} = 70^{\circ}\text{C}$	69	A
I_T	Continuous (direct) on-state current	$T_{case} = 85^{\circ}\text{C}$	57	A

ACR44U

SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) forward current	10ms half sine: $T_{case} = 125^{\circ}\text{C}$	550	A
I^2t	I^2t for fusing		1500	A ² s

THERMAL AND MECHANICAL DATA

Symbol	Parameter	Conditions	Min.	Max.	Units
$R_{\theta(j-c)}$	Thermal resistance - junction to case	d.c.	-	0.35	$^{\circ}\text{C}/\text{W}$
$R_{\theta(c-h)}$	Thermal resistance - case to heatsink	Mounting torque 3.5Nm with mounting compound	-	0.25	$^{\circ}\text{C}/\text{W}$
T_{vj}	Virtual junction temperature	On-state (conducting)	-	125	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		-55	125	$^{\circ}\text{C}$
-	Mounting torque		3.5	4.0	Nm

DYNAMIC CHARACTERISTICS

$T_{case} = 125^{\circ}\text{C}$ unless otherwise stated.

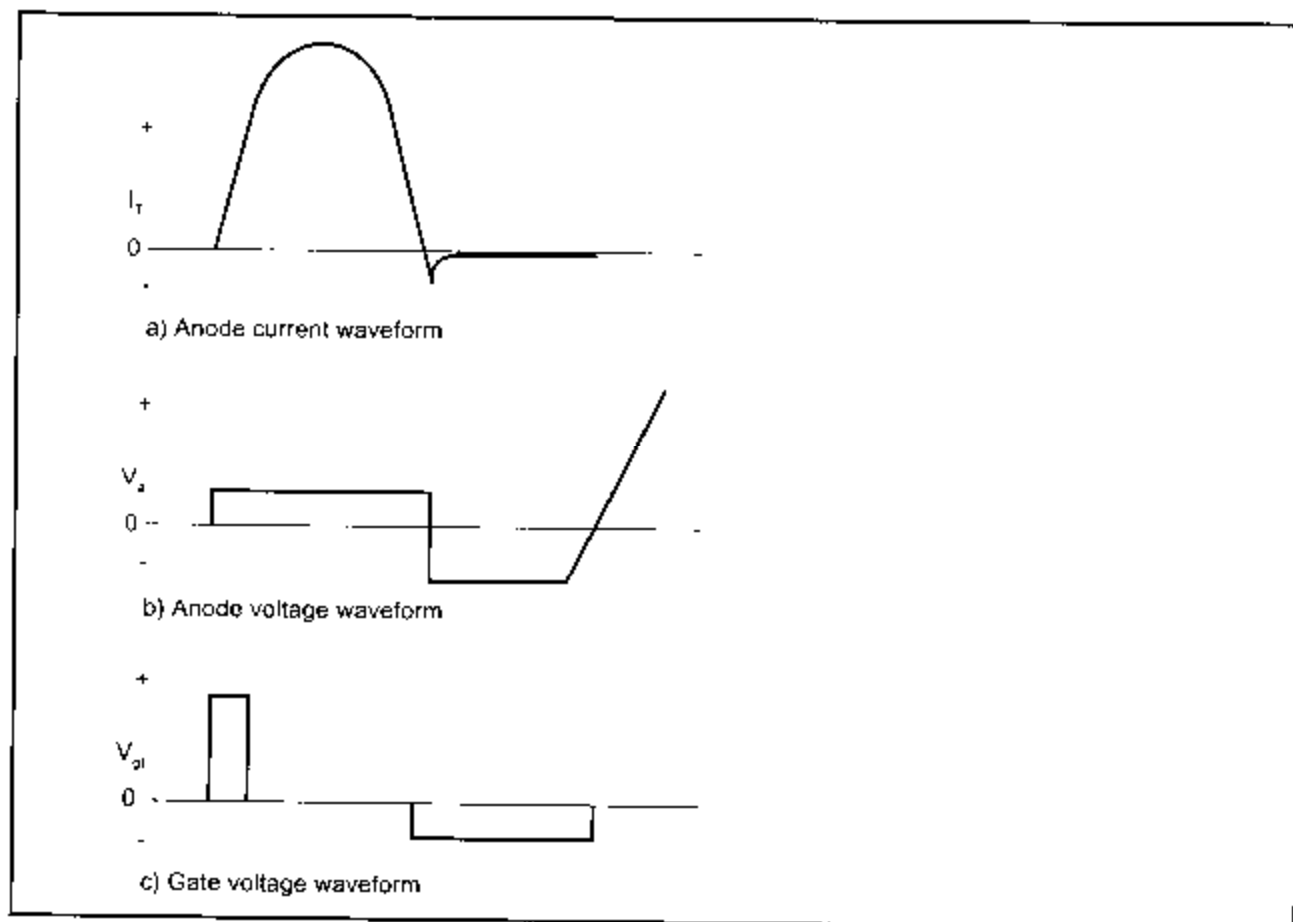
Symbol	Parameter	Conditions	Typ.	Max.	Units
V_{TU}	Maximum on-state voltage	At 100A peak, $T_{case} = 25^{\circ}\text{C}$	-	2.7	V
I_{RM}/I_{DRM}	Peak reverse and off-state current	At V_{DRM}/V_{DRM} , $T_{case} = 125^{\circ}\text{C}$	-	20/10	mA
dV/dt	Maximum linear rate of rise of off-state voltage	To V_{DRM} , $T_j = 125^{\circ}\text{C}$, gate open circuit	-	600	V/ μs
dI/dt	Rate of rise of on-state current	From V_{DRM} to 125A. Gate source 15V, 15 Ω $t_f = 50\text{ns}$	-	2000	A/ μs
V_{TTC}	Threshold voltage	-	-	1.5	V
r_l	On-state slope resistance	-	-	13.3	m Ω
I_L	Latching current	-	120	-	mA
I_H	Holding current	-	25	-	mA
t_d	Delay time	$V_o = 300\text{V}$, gate source = 15V, 15 Ω	-	250	ns
t_v	Turn-off time (with antiparallel diode)	$I_f = 50\text{A}$, square wave $t_o = 50\mu\text{s}$, $T_j = 120^{\circ}\text{C}$, $dI_f/dt = 50\text{A}/\mu\text{s}$, $dV/dt = 600\text{V}/\mu\text{s}$ to V_{DRM} , gate voltage at turn-off 3.5-4.5V, $V_R = -1\text{V}$	-	6.0	μs

* Available to 1000V/ μs .

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Conditions	Typ.	Max.	Units	
V_{GT}	Gate trigger voltage	$V_{DWM} = 12V, R_g = 30\Omega, T_{case} = 25^\circ C$	0.9	3.0	V	
I_{GI}	Gate trigger current	$V_{DWM} = 12V, R_g = 30\Omega, T_{case} = 25^\circ C$	60	200	mA	
V_{FGM}	Peak forward gate voltage	-	-	40	V	
V_{RGM}	Peak reverse gate voltage	-	-	10	V	
I_{FGM}	Peak forward gate current	-	-	10	A	
P_{GM}	Peak gate power	-	-	40	W	
P_{GAV}	Average gate power	Average time 10ms max	Forward	-	10	W
			Reverse	-	6	W

WAVEFORM OF GATE VOLTAGE AT TURN-OFF



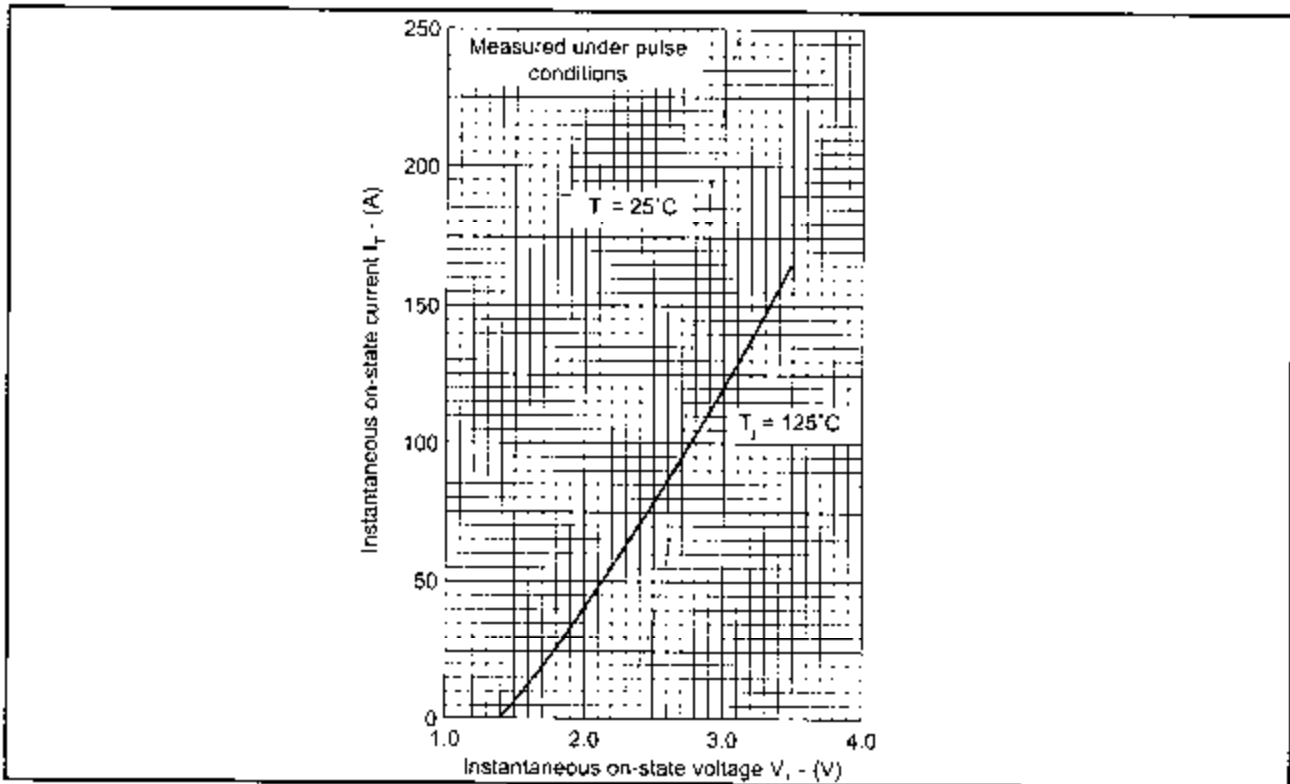


Fig.1 Maximum (limit) on-state characteristics

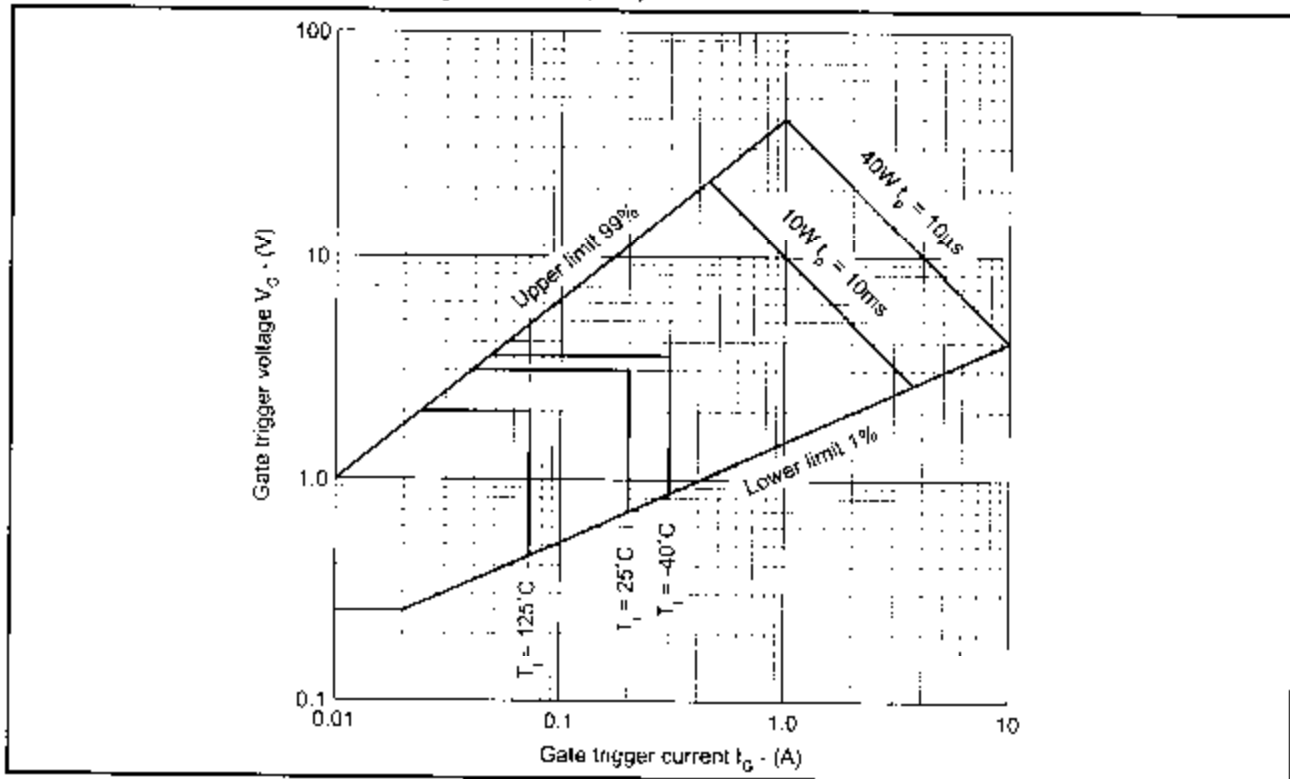


Fig.2 Gate characteristics

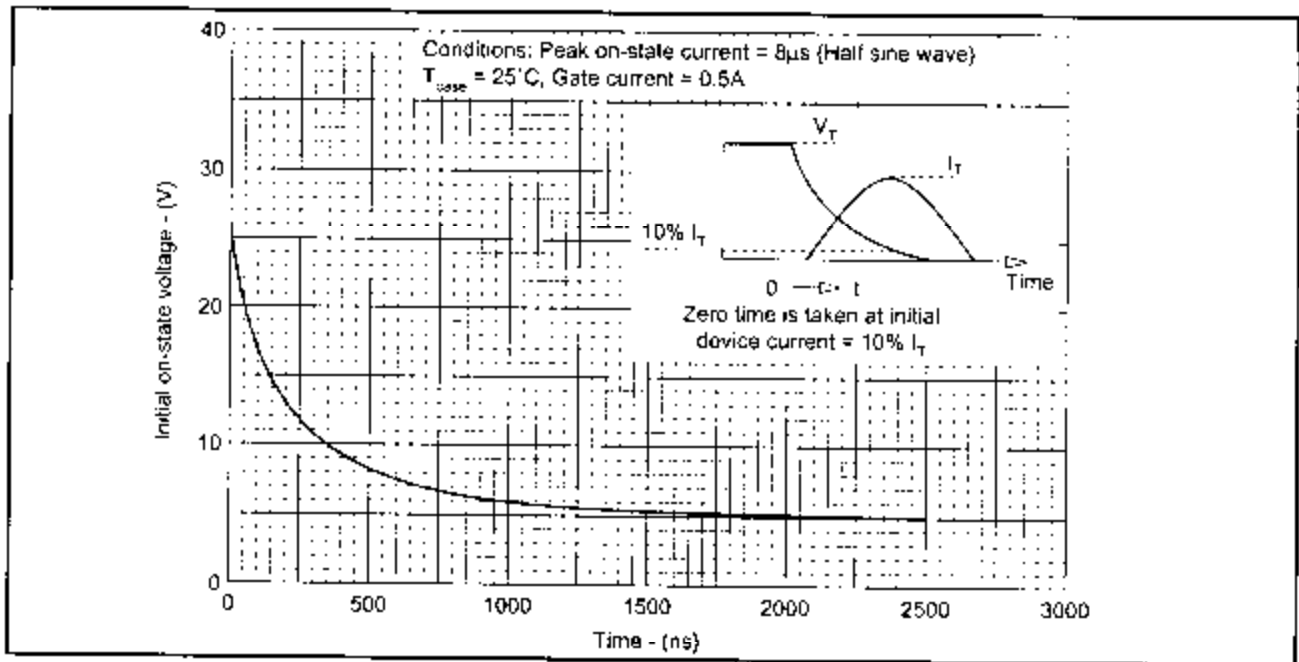


Fig.3 Typical initial on-state voltage vs time

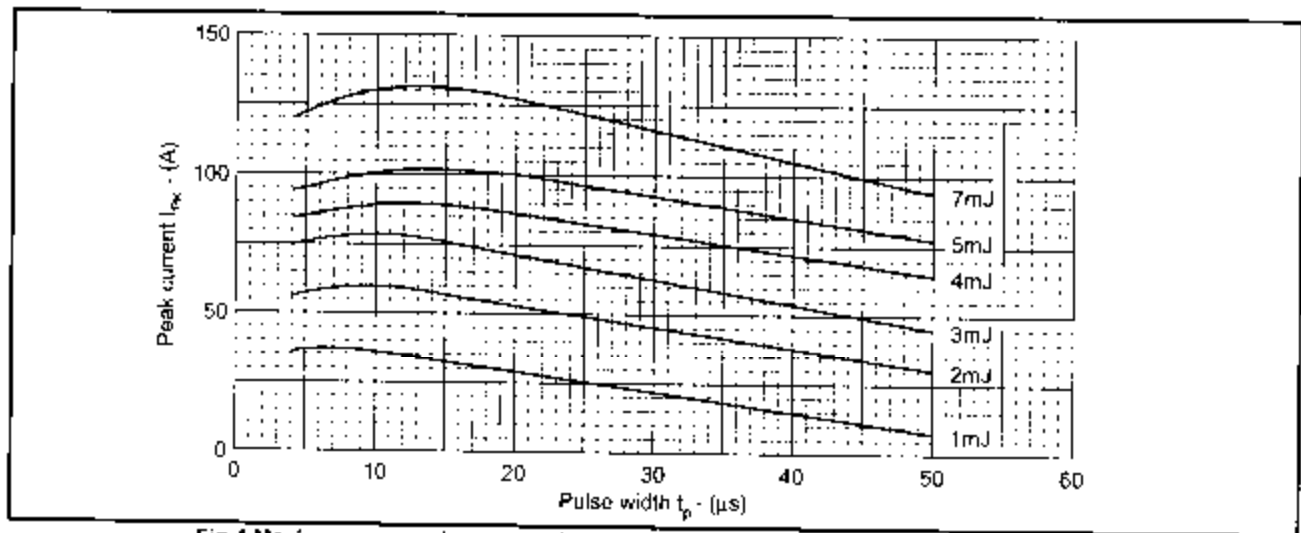


Fig.4 Maximum energy loss per pulse when switching a half sinusoidal pulse from 600V

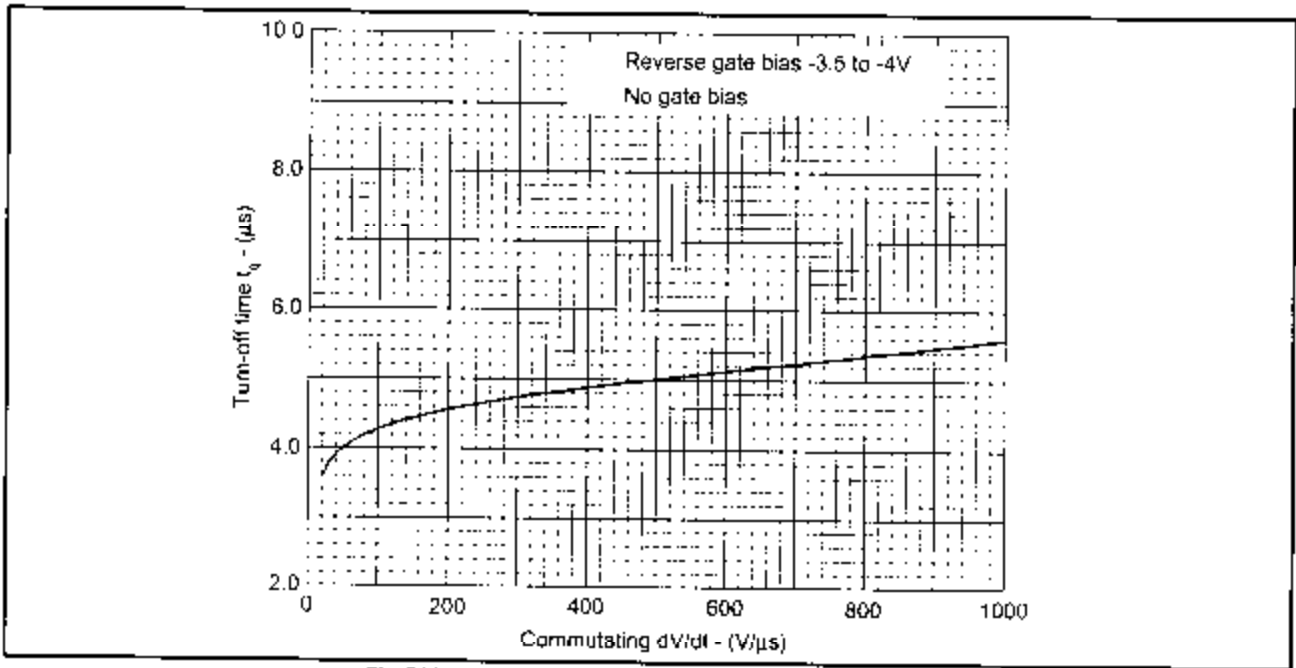


Fig.5 Variation of turn-off time with commutating dv/dt

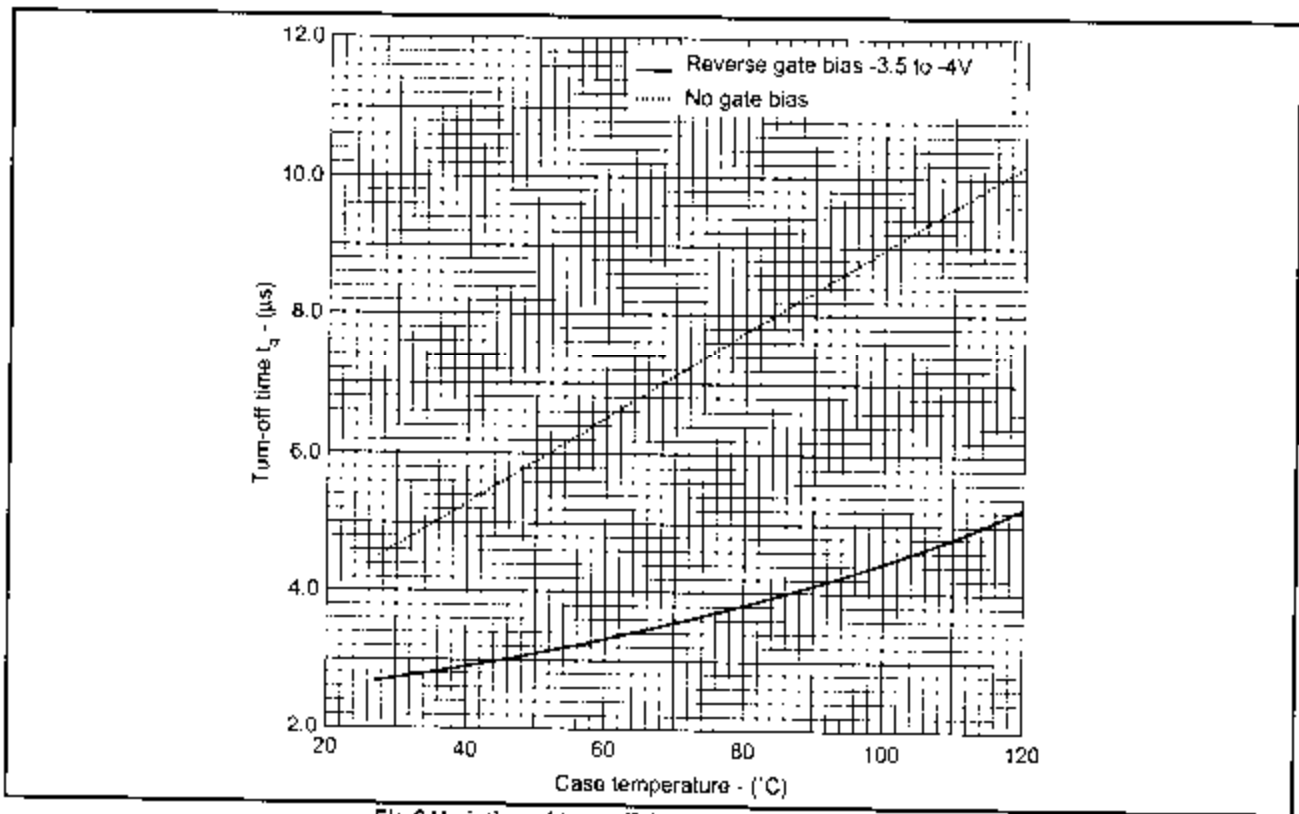
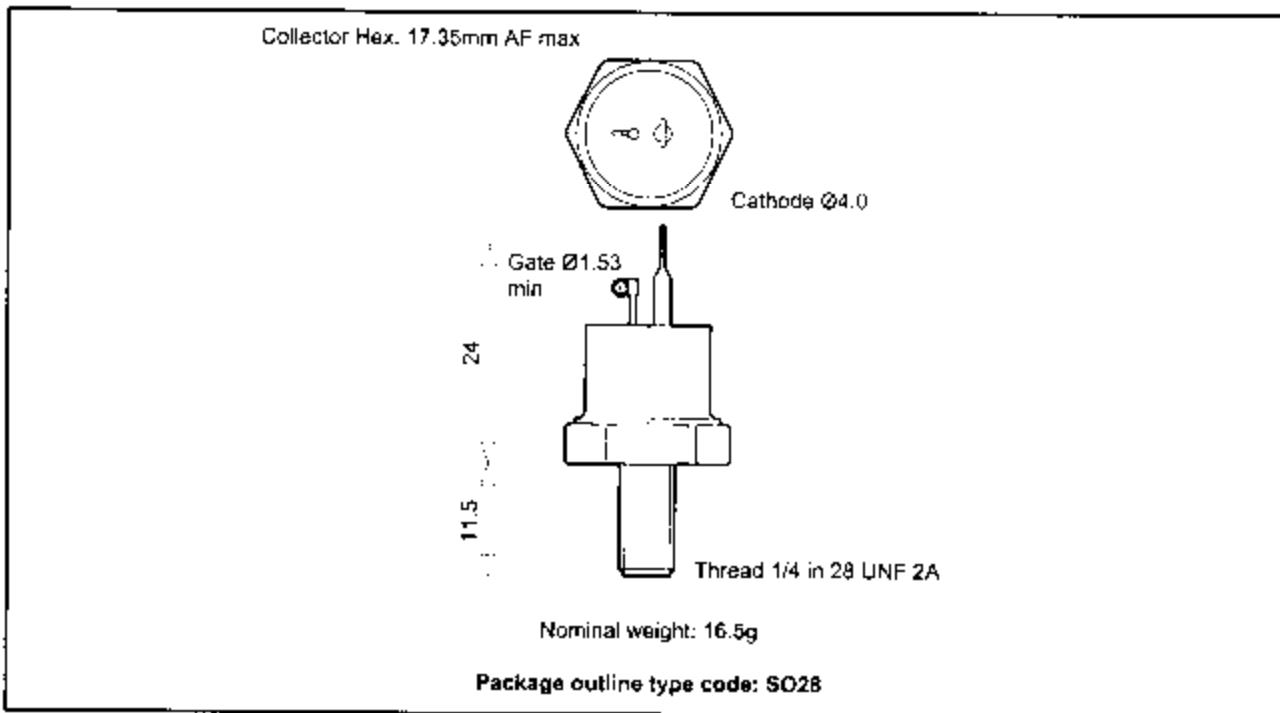


Fig.6 Variation of turn-off time with case temperature

PACKAGE DETAILS

For further package information, please contact your local Customer Service Centre. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



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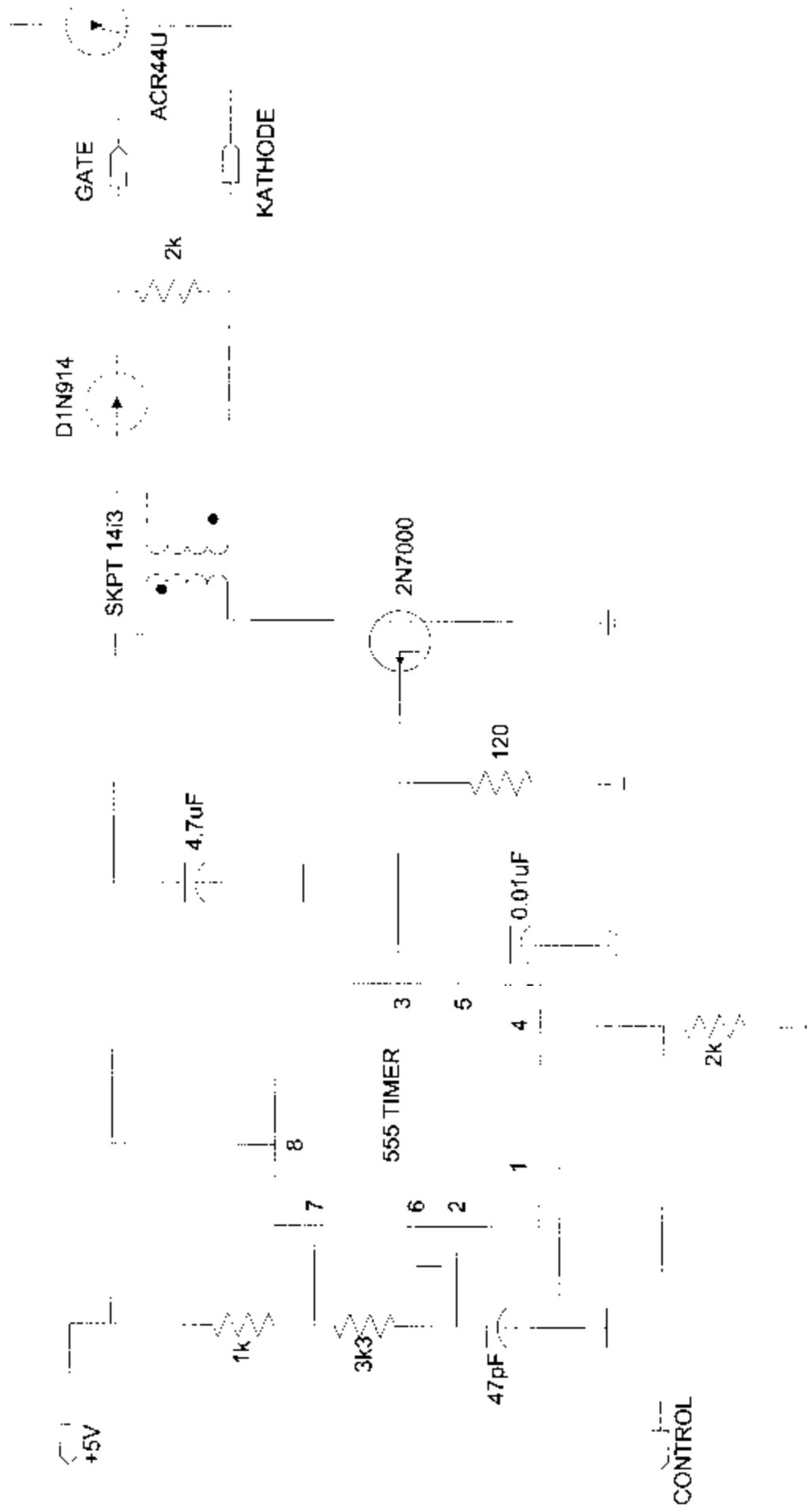
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ACR44U 12LE GATE DRIVE CIRCUIT



APPENDIX B : INVERTER SYSTEMS STUDIES

- I. OPEN LOOP FOURIER ANALYSIS EQUATIONS
- II. OPEN LOOP FOURIER ANALYSIS RESULTS
- III. BATTERY BACKUP SIMULATION

The fourier series for the open loop signal has the form:

$$f(t) = \sum_{n=1,3,5}^{\infty} (b_n * \sin(2\pi n f_0 t))$$

where

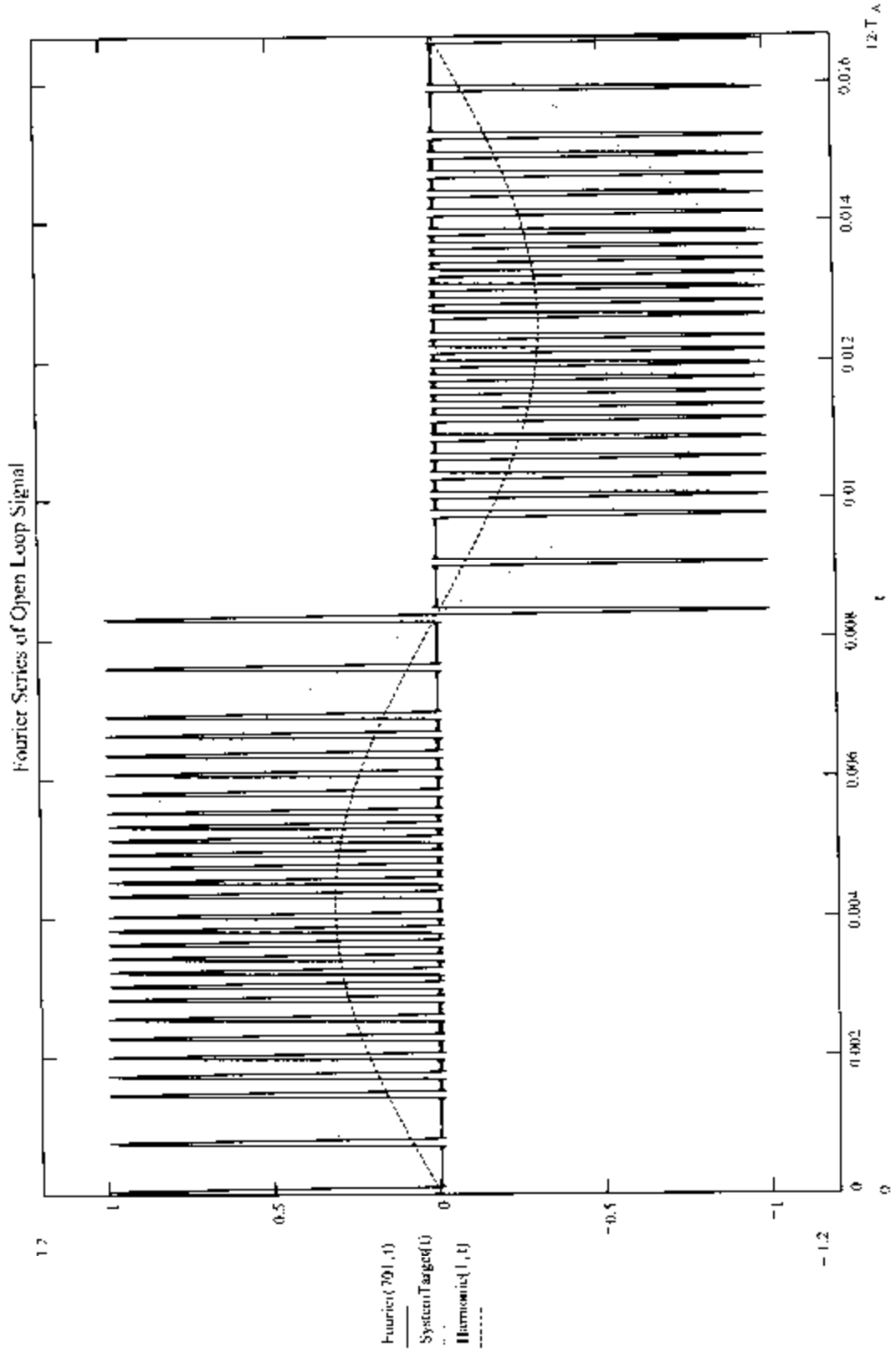
$$b_n = \frac{(4 * V_r * f_r * f_0)}{\pi * (f_r^2 - (n * f_0)^2)} * \left[\sum_{k=0}^{K_n-1} \left(\sin \left(2\pi n f_0 * \left(\frac{k}{f_1} \right) \right) + \sin \left(2\pi n f_0 * \left(\frac{k}{f_1} + \frac{1}{2f_1} \right) \right) \right) \right. \\ \left. + \sum_{k=0}^{K_n-1} \left(\sin \left(2\pi n f_0 * \left(\frac{k}{f_1} + T_d \right) \right) + \sin \left(2\pi n f_0 * \left(\frac{k}{f_1} + \frac{1}{2f_1} + T_d \right) \right) \right) \right] \\ \left. + \sum_{k=0}^{K_n-1} \left(\sin \left(2\pi n f_0 * \left(\frac{k}{f_1} + 2T_d \right) \right) + \sin \left(2\pi n f_0 * \left(\frac{k}{f_1} + \frac{1}{2f_1} + 2T_d \right) \right) \right) \right]$$

and $f_0 = 60\text{Hz}$, $f_r = 20\text{kHz}$

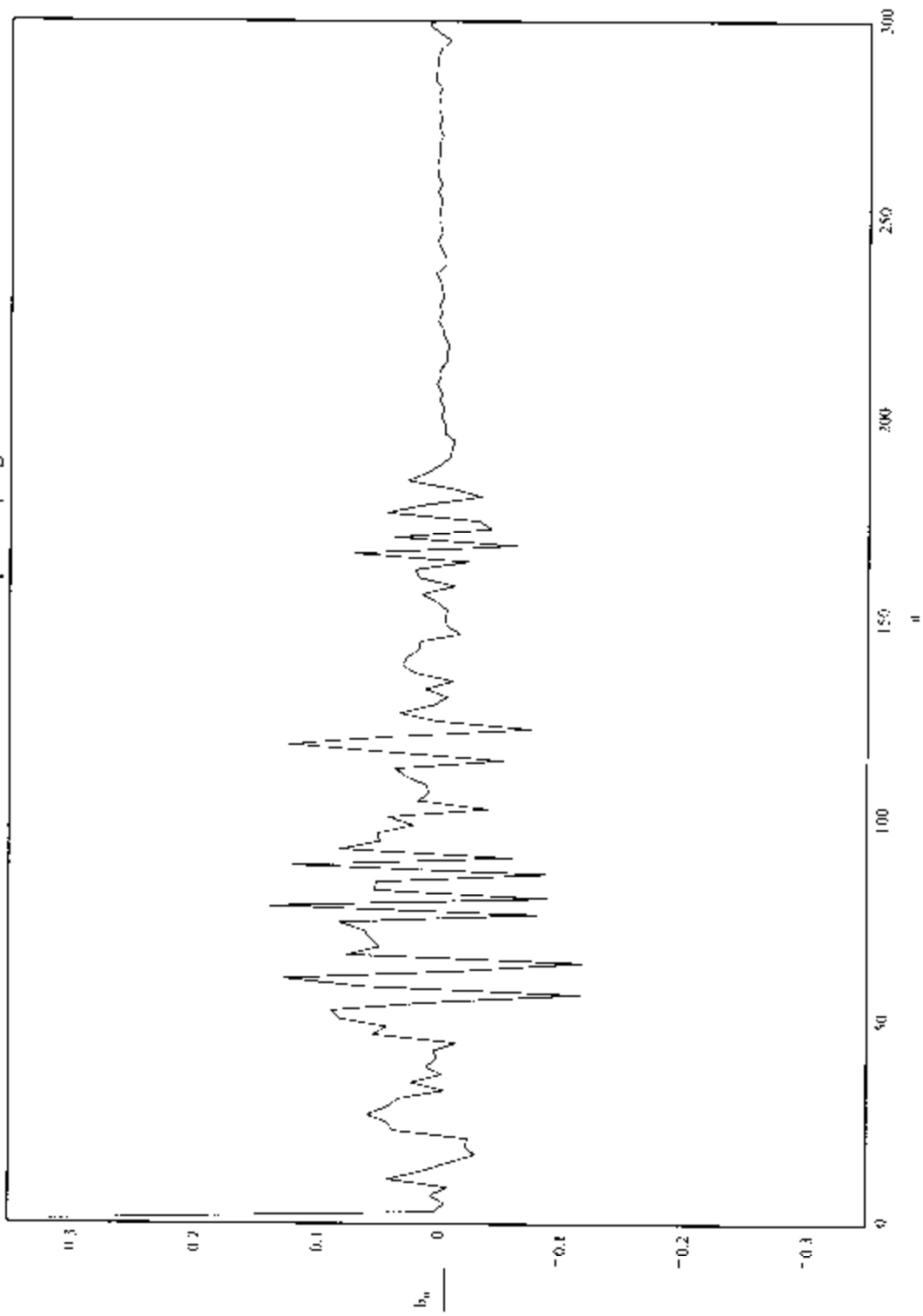
T_d Width of modulation period

K_n Number of pulses within modulation period

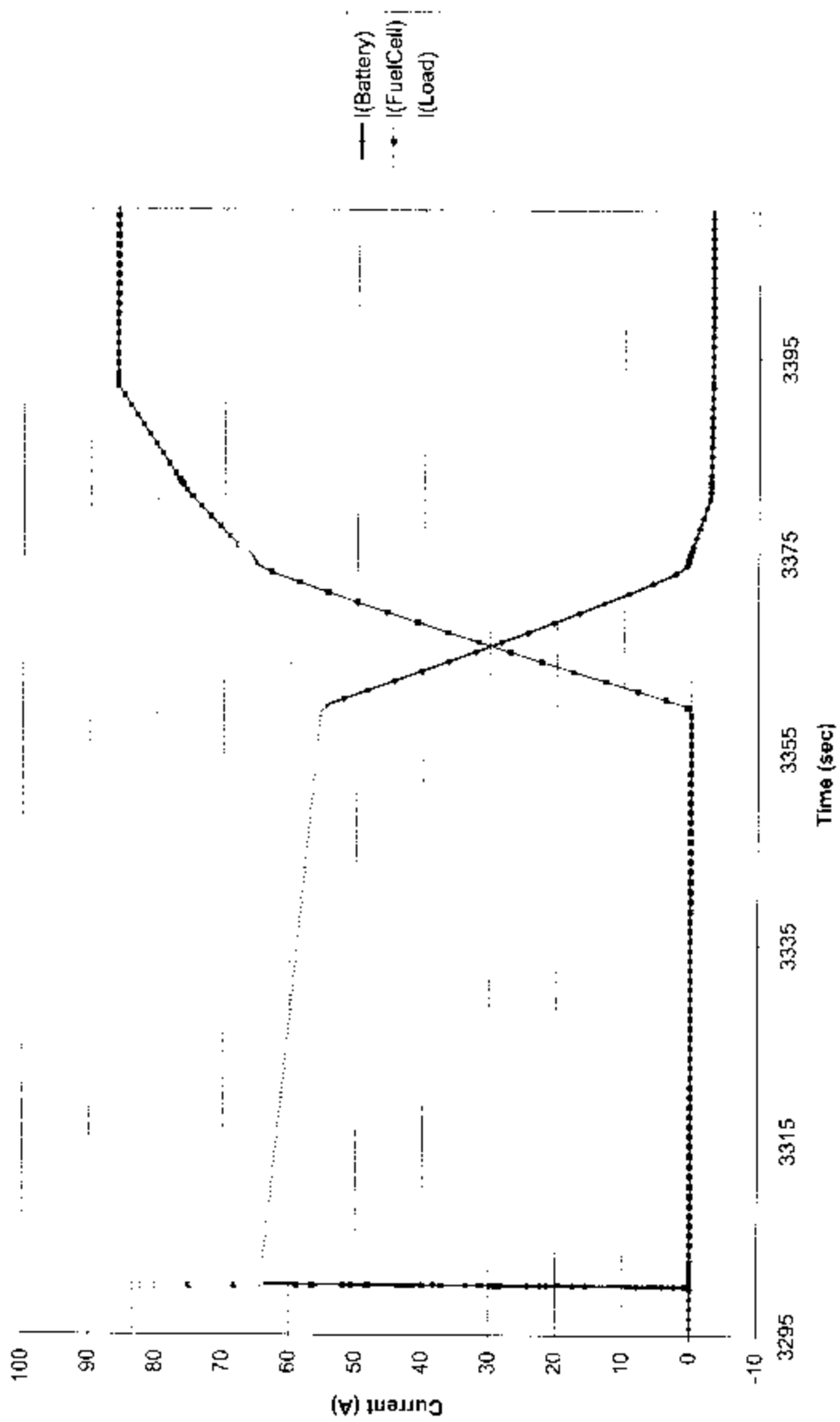
$f_n = \frac{K_n}{T_d}$, the modulation frequency



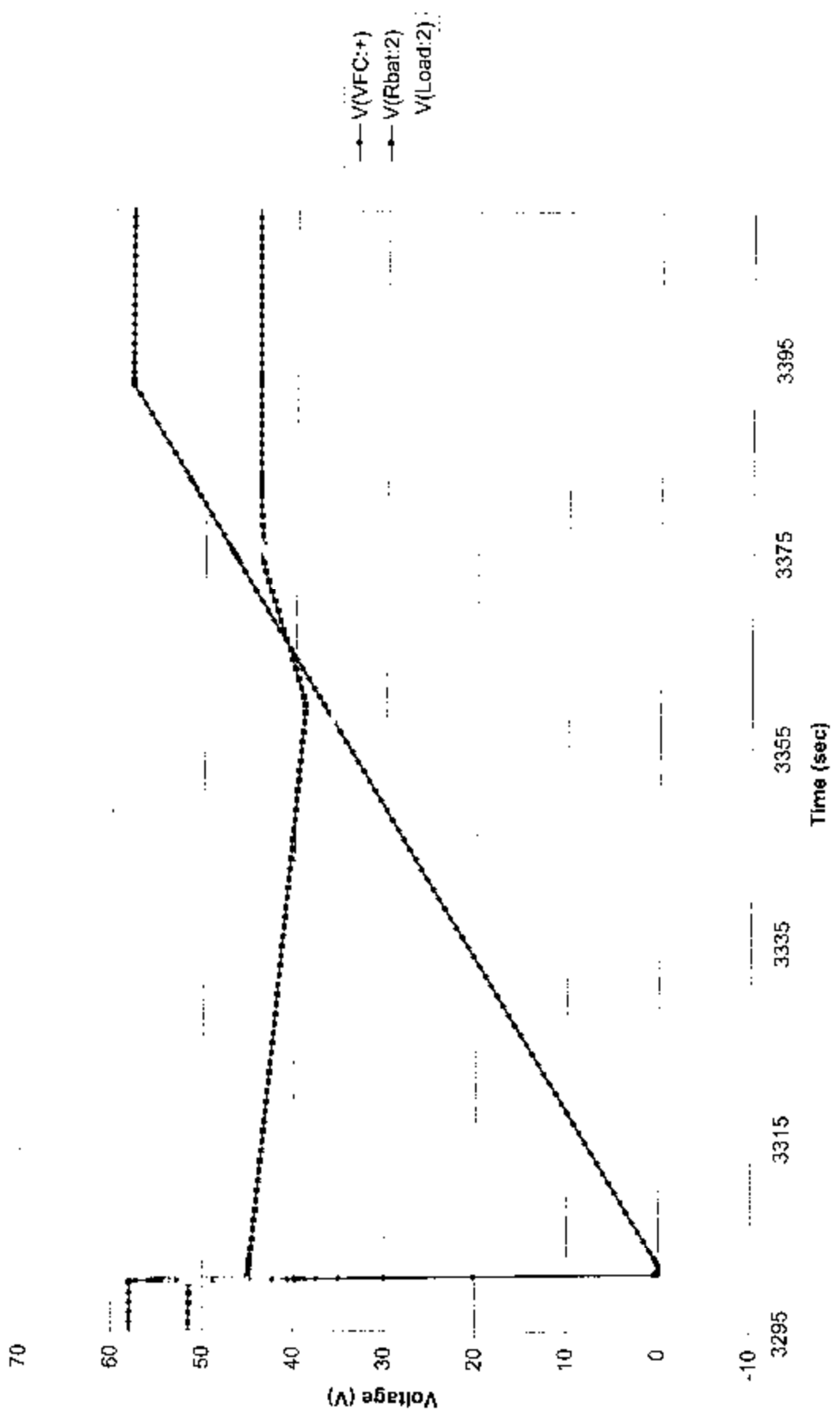
Fourier Coefficients of Open Loop Signal



System Currents For One Load Transient Cycle



System Voltages For One Load Transient Cycle



APPENDIX C: COST ANALYSIS SPREADSHEETS

- I. SENIOR DESIGN COST ANALYSIS
- II. ESTIMATED PROTOTYPE COST @ 10kW

APPENDIX D: GLOSSARY OF TERMS

<u>Fuel Cell</u>	An electrochemical device that converts chemical energy directly to electrical energy
<u>Gate Driver</u>	Circuitry that transforms logic level voltages to voltages necessary to operate the gate of power electronic devices
<u>Harmonic Distortion</u>	Distortion caused by resonance in multiples of a circuit's natural frequency
<u>IGBT Transistor</u>	Insulated Gate Bipolar Transistor
<u>Inverter</u>	An electrical device that converts direct current to alternating current
<u>LC Circuit</u>	A circuit made of inductors and capacitors
<u>Lowpass Filter</u>	A filter that passes energy at low frequencies
<u>Matrix Converter</u>	An externally controlled rectifier
<u>MOSFET Transistor</u>	Metal Oxide Semiconducting Field Effect Transistor
<u>Pspice</u>	Analog and Digital circuitry simulator
<u>Pulse Width Modulation</u>	A method of reducing voltage by switching the source voltage off and on in pulses of varying lengths
<u>Pulse Density Modulation</u>	A method of reducing voltage by switching the source voltage off and on in pulses that vary in spacing
<u>Series Resonant Converter</u>	A switched LC circuit that converts DC voltage to AC
<u>Thyristor</u>	A type of power transistor, having 3 p-n junctions
<u>Waveform Conditioning</u>	Circuitry that changes an input waveform to an ideal output waveform